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Voor lidmaatschap wende men zich tot de secretaris. Het lidmaatschap staat -behoudens ballotage- open voor academisch gegradueerden en hen, wier kennis of ervaring naar het oordeel van het bestuur een vruchtbaar lidmaatschap mogelijk maakt. De contributie bedraagt fl. 55,--.

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De examens door het Genootschap ingesteld en afgenomen zijn:

a. op lager technisch niveau:"Elektronica monteur NERG"
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DEVICES FOR SIGNAL PROCESSING

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ABSTRACT

With the advent of LSI technology, signal processing hardware and software is slowly changing into dedicated IC's. A few examples are given in this paper, considering a TV-ghost cancellation circuit a portable reading wand and a speech processing system. Interesting is the fact that large systems which were totally unconceivable because uneconomical before the advent of LSI technology,now are being seriously considered for consumer and other applications.

INTRODUCTION

Future telecommunication systems, data acquisition and transmission systems will draw heavily upon LSI and VLSI. It is quite obvious that microprocessors as well as dedicated IC's will share the job. The advent of high performance MOS compatible analog-digital circuits however, is an incentive to develop an ever increasing number of custom designed IC's. Hence devices for signal processing are emerging which are based on innovative designs using CCD's, transversal filters, recursive filters op amps, A/D and D/A converters, etc. Rather than trying to seize the phylosophy behind this evolution, some typical examples will be examined.

TV GHOST CANCELLATION CIRCUIT

TV reception may be disturbed by spurious reflections which cause ghost images on the screen. The elimination of single undistorded echos may be achieved by means of an echo cancellation circuit which basically consists of a recursive CCD filter generating an artificial echo with the same delay and opposite polarity (1). The delay element for this application of course is a CCD line, clocked at an adjustable frequency. When properly time-set and with adequate amplitude of the delayed signal, exact cancellation of the unwanted echo can be achieved. A bloc diagram of the circuit is shown in fig. 1. Delay and gain adjustments of course must be set automatically. The TV synchronization signal during the field retrace period is used for this purpose as a test signal. Fig. 2a shows a single undistorded echo affecting the synchronization signal. Clamping the signal at the very beginning of the unit step and compairing it with the mean level of the unit step during the "sample" period, yields a measure of the echo's amplitude. The output signal of the comparator controls an up-down counter which provides a DC gain control signal to adjust the amplitude of the CCD output signal in order to equalize sample and clamp signals. It should be pointed out that before the correct amplitude adjustment is found, multiple reflexions appear which result from the recursivity of the filter (fig. 2b). This explains why the sample period is taken at the end of the sync. pulse.

Once the amplitude correctly set, the delay adjustment must be achieved. As long as overlapping of the echo versus the CCD signal occurs, or vice-versa, a series of pulses is generated whose polarity refered to the echo determines without ambiguity whether the CCD delay should be lenghtened or shortened.

The same principle was also applied to 2-wire full-duplex data transmission systems (2).

AUTOMATIC CHARACTER READING

In supermarkets, hospitals, libraries, reading wands can fulfil the need for fast and reliable data transcription from labels into other storage media, like magnetic tape or computer memory. Portability and cheapness are requirements which can be met satisfactorily by means of LSI implementation. Reading wands consist of a retina on which the image of a character is focused plus additional recognition circuitry. The retina may be a two dimensional CCD imager or a photodiode array (3). Single rows of photoelements are less attractive for the actual scanning speed of operators is unknown, unless mechanically probed.The recognition algorithm of course must be a simple one but it may be strongly dependent on the kind of material to be read. E.g. standard single font characters may well be recognized by means of a simple set of masks even when printing quality is not good. Multifont or handprinted characters however, may be recognized preferably on the basis of a topological analysis, thus are more demanding. An example of a feature extraction scheme is considered hereafter in which the recognition hardware consists of an LSI circuit with a microprocessor. The LSI circuit performs several repetitive preprocessing functions leaving the more refined feature extraction algorithms to the latter (4).

Binarisation of the image occurs when a full character is sensed by the retina. Isolated black dots and gaps in the tracing of the character first are removed by means of a separate IC (fill and delete). The subsequent image is stored in the memory of a contour analysis LSI where it is explored by means of a 2 x 2 squares contour detection window that searches for the character, locks onto the boundary and then is constrained to follow the edge of the pattern as described in fig. 3a. Decisions are taken concerning the tangent vector slope among eight quantized values multiple of $\pi/4$ (5) and the subsequent window displacements in order to effectively track the boundary. The motion can be compared to the behaviour of a roller constrained to follow the character edge acting as a fixed cam. Context analysis is performed simultaneously. According to the value of the 12 squares surrounding the 2 x 2 contour detection window, black dots belonging to the character outer edge may be deleted or not.

Turning three or four time around the pattern provides complete character peeling (fig. 3c).The resulting string of 3 bit-coded vectors describing the contour of the skeletonized character (fig. 3d) is fed to the microprecessor for further analysis and feature extraction. These include branches and loops extraction, filtering, curvaturve determination, etc. leading to final classification of the character and the availability of its ASCII code at the system output.

Fig. 4 shows the block diagram of the edge and skeleton detection MOS circuit. It consists of a 32 x 24 dynamic one-transistor-per-cell RAM matrix. This memory is addressed accordingly to the actuel content of the previous 2 x 2 contour detection window.

Four adjacent columns among the parallel outputs of the RAM amplifiers are selected by means of a ROM matrix in order to reconstitute the four 4-bit words necessary to check the values of the 2 x 2 window and its neighbourhood. These words feed the central unit which provides simultaneously a vector tangent to the boundary, incremental instructions for the X and Y counters, internal timing and the central unit decoder address and memory rewriting signal when a black dot must be deleted at the character periphery. The X and Y counter-decoder stages must accomodate to various incremental instructions like +2, +1, +0, -1. The skeletonization and line-follower random logic is easily implemented using a Programmable Logic Array (PLA). The versatility required from the counters makes PLA's more useful too for the scanning of the RAM matrix along both X and Y directions.

The experimental 3000-transistor circuit of fig.4 was fabricated using p-channel depletion load technology. Contour detection and thinning are performed in about 4msec leading to a global reading speed of 100 characters/sec. Continously deformed or handprinted characters are successfully recognized by the system with broad tolerances on the over-all sizes and thicknesses of the input patterns.

VOCODERS

It is a well known fact that speech is a compressible source of information. Data rates as low as 50 to 70 bits/s have been measured when the speech signal was restricted to the textual context of utterances. We are interested however in auditory hints such as speaker's identity, etc. Hence, higher bit rates are required and most attempts to encode speech signals presently are based upon a min of 1000 bits/s.

Speech encoding furthermore, is raising a considerable amount of interest in view of PCM communications. Codecs already have been implemented successfully in I.C. form (6) and flow control procedures, such as packet switching, are becoming important research topics to help traffic decongestion. Similarly, the possibility to integrate channel Vocoders is seriously considered by I.C. manufacturers (7).

The channel Vocoder, invented by Homer Dudley in the 1930's, is a speech analysis system which is supposed to extract essential features from the speech signal such as :

1) is the signal quasi periodic (e.g. a vowel) or a voiceless sound (e.g. a "sh" or a "f") ?
2) if the signal is periodic, estimate pitch and vocal-tract (fig. 5).

Voiceless sounds can be crudely parametized in terms of noise. Sustained vowels require spectral analysis tools to extract pitch and vocal-tract (fig. 6). In the Vocoder, a bank of narrowband filters is used in order to achieve spectral analysis. The actual bandwidths of the filters is the result of a compromise. If the bandwidths are very small (5 to 10 Hz) and if numerous filters are spaced very closely (e.g. 300 filters), a good spectral signature is obtained which yields both vocal-tract and pitch information. In the other case, when rather large bandwidths are considered (e.g. 100 Hz) a smooth spectrum is obtained that encompassed several harmonics and pitch information is lost. In the first case, a prohibitive number of filters and the difficulty to separate pitch and vocal-tract make this method useless for integration. In the second case, only a small number of filters is sufficient (e.g. 20 filters) but another algorithm must be looked at to recover pitch information. One is known as the Gold-Rabiner algorithm. It is a time domain method which consists to measure the time intervals between adjacent peaks and valleys of the speech waveform wherefrom the pitch is statistically estimated.
A channel Vocoder based on this principle is illustrated in fig. 7 and its implantation on a single I.C. is under way. The circuit comprises 19 narrow-band CCD transversal filters with bandwidths ranking from 120 Hz to 500 Hz. Their outputs are fully rectified and log sampled every 20 mS. This results in 39 bits vocal-tract information, to which 7 more bits must be added in order to restore pitch information, and 2 additional control bits for voiced-unvoiced decision, etc. The total bit stream (48 bits every 20 mS) amounts to 2.4 kbits/s.

Pitch tracking seems to be the most difficult circuit to integrate. Several different approaches are being considered among which cepstrum evaluation perhaps may bring a satisfactorily answer. The cepstrum heavily draws upon the existence of Fast Fourier Transforms wich have already been implemented in IC form (8). The basic idea behind this can be understood from the following expression of the Fourier transform :

$$F(j\mu t) = \underbrace{e^{-j\frac{\mu t^2}{2}}}_{\text{postmultiply}} \cdot \underbrace{\int_{-\infty}^{+\infty} \underbrace{f(p) e^{-j\frac{\mu t^2}{2}}}_{\text{premultiply}} \cdot e^{+j\frac{\mu t^2}{2}(p-t)^2} dp}_{\text{convolve}}$$

Where $F(j\mu t)$ represents the Fourier transform of $f(t)$.
The factor $\exp\left(\pm j\frac{\mu t^2}{2}\right)$ which appears three times above is characteristic of chirp filters which can be implemented easily by means of CCD transversal filters.

$\mathrm{Exp}\left(\pm j\frac{\mu t^2}{2}\right)$ in fact represents a vector of constant length rotating at a linearly varying speed. Consequently it does represent a linearly frequency modulated sine or cosine wave. The above expression can be viewed as shown in fig. 8. where premultiplication is achieved by means of a multiplying D to A converter (9), convolution is done by means of a chirp Z CCD transversal filter, and postmultiplication is similar to premultiplication. Notice that when the power spectrum only is required, postmultiplication may be omitted. Hence the circuit may be simplified as shown in fig. 9 representing the bloc diagram of an I.C. which is commercially available.

Let us now examine how pitch extraction effectively can be achieved by means of the Cepstrum which may be defined as (10).

$$C(t) = \left|FT(\log\left|FT\ f(t)\right|^2)\right|^2$$

FT represents the Fourier Transform. Accordingly to this expression the cepstrum is the power spectrum of the log power spectrum of the speech signal. It may be considered as a cascade of two of the above IC's with a log transformation in between. Just to get some physical insight let us consider a simple example consisting of a periodic square wave (fig. 10a) whose power spectrum follows

the well known $(\sin\omega t^2)/(\omega t)^2$ law (fig. 10b). Taking the log of the power spectrum results in a modified spectral signature in which the importance of the smaller lobes has been emphasized relatively to the larger ones (fig. 10c). Considered as a time domain signal, the output signal of the chirp Z Fourier Transform circuit, resembles to the transient response of a band pass filter. Thus, after a second FT has been computed, we obtain a peak somewhere in the time domain (called quefrency) which is representative of the harmonics spacing of the first FT. Hence pitch detection and evaluation may be drawn from the cepstrum provided a window is used which eliminates the low quefrency components of the Ceptrum.

Another approach which perhaps is more powerful, is the computation of the complex cepstrum which is not subject to the loss of phase information like the power cepstrum. A slightly different approach is used here, since the computation of the complex cepstrum is based on a first FT, then a log conversion, then an inverse FT. At this point, pitch information again is available in the form of a sharp peak while the vocal-tract information is concentrated in the lower part of the cepstrum. Following this another FT of the windowed vocal-tract is used to obtain directly a smooth spectral signature.

Voice synthesis IC's must be used in order to restore the speech signal. Some applications however resume to the synthesis aspect only. This is the case for talking devices such as a talking calculator which is being developed for blind persons. In this application, the speech information is frozen in a ROM-like memory which is addressed accordingly to the spoken numbers. As IC consisting of a bank of variable size capacitors loaded to the same voltage and sequentially addressed has been developped for this purpose (11).

CONCLUSION

The potentialities of LSI technology today and VLSI tomorrow enable system engineers to integrate sophisticated systems on a single chip,opening many new wide areas of applications. Not only an increasing number of existing systems is being implemented in IC's, but many new ones which were believed to be impractical for economical reasons, are slowly emerging accordingly to new consumer areas which have been identified. This situation is clearly evidenced in telecommunications where much signal processing hardware and software now is being implemented into devices for signal processing. Most interesting is the fact that these devices very often are based on entirely new algorithms which are not the obvious successors of the existing ones. In other words, the design of advanced dedicated IC's for signal processing perhaps is becoming a more challenging problem from the viewpoint of system design than from that of circuit design. IC systems engineers will need increasingly to be aware of the existence of many new interesting algorithms and, overal, they should be imaginative.

REFERENCES

(1) H.W. Hanneman and B. Visser.
An experimental TV ghost cancellation circuit with automatic gain control.
CCD conference record, 1976 Edimburgh.

(2) H.C. Van den Elzen, P.J. van Gerwen, W.A.M. Snijders.
Echo cancellation in a 2-wire full-duplex data transmission system with bipolar encoding.
NTC conference 1976, Dallas, Texas.

(3) P.Jespers, F.Van de Wiele, M.H.White.
Solid State Imaging
Noordnoff Int. Publishing, Leyden
Series E : Applied Science, n° 16.

(4) M.Rahier, P.Jespers.
A low-cost hand-carried OCR system implemented with monolithic IC's.
The 4th InternationalJoint Conference on Pattern Recognition - Nov. 7-10, 1978, Kyoto - Japon.

(5) H.Freeman.
On the encoding of arbitrary geometric configuration.
IRE Trans on Electronic Computers, June 1961.

(6) J.Compeers, H.De Man.
Nonuniform pulse code modulation encoder using double polysilicon technology.
IEEE Journal of Solid State, specialissue on ESSCIRC 1977, June 1978.

(7) B.Gold.
Digital Speech Networks.
Proc. of IEEE, vol. 65, n° 12, Dec. 1977.

(8) D.D.Buss, R.W.Brodensen, C.R.Hewes.
Charge coupled devices for Analog Signal Processing.
Proc. of IEEE, vol. 64, n° 5, May 1976.

(9) J.F. Albarran D.Hodges.
A charge transfer multiplying digital-to-analog converter.
IEEE Intern. Solid State Circuit Conference Digest of Technical Papers 1976.
p. 202-203.

(10) M.A.Jack, P.M.Grant, J.H.Collins.
Waveform detection and classification with SAW Cepstrum Analysis.
IEEE Trans on Aerospace and Electronic Systems.
Vol. AES-13, n° 6, nov. 1977.

and A.M.Noll.
Short-time Spectrum and Cepstrum Techniques for Vocal-pitch detection.
Journal of Acoustical Soc. of America, vol 36, n° 2, febr. 1964.

(11) E.Bruun, Ole Olesen.
Analog Capacitance ROM with IGFET Bucket-Brigade Schift Register.
IEEE Journal of Solid State Circuits, vol. SC 10, n° 1, febr. 1975.

Invited paper at Esscirc 78
September 1978 in Amsterdam

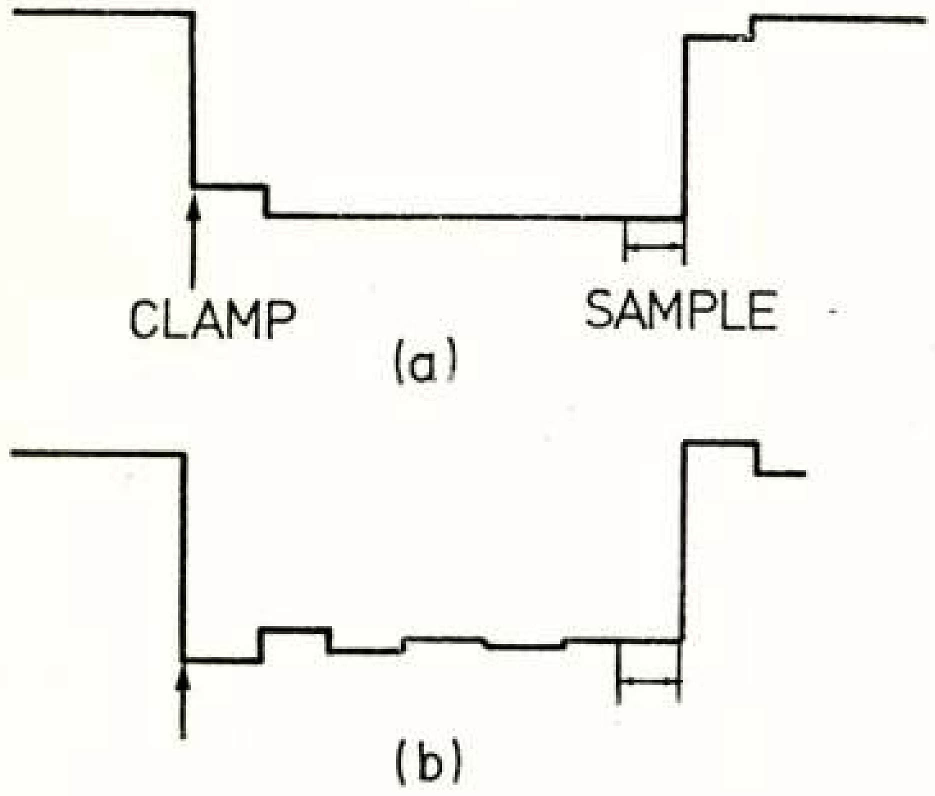


Fig. 1

a) Use of sync. signal during the field retrace period in order to adjust amplitude and delay of the echo cancellation circuit.

b) When improperly set, the CCD recursive filter generates a series of unwanted echos.

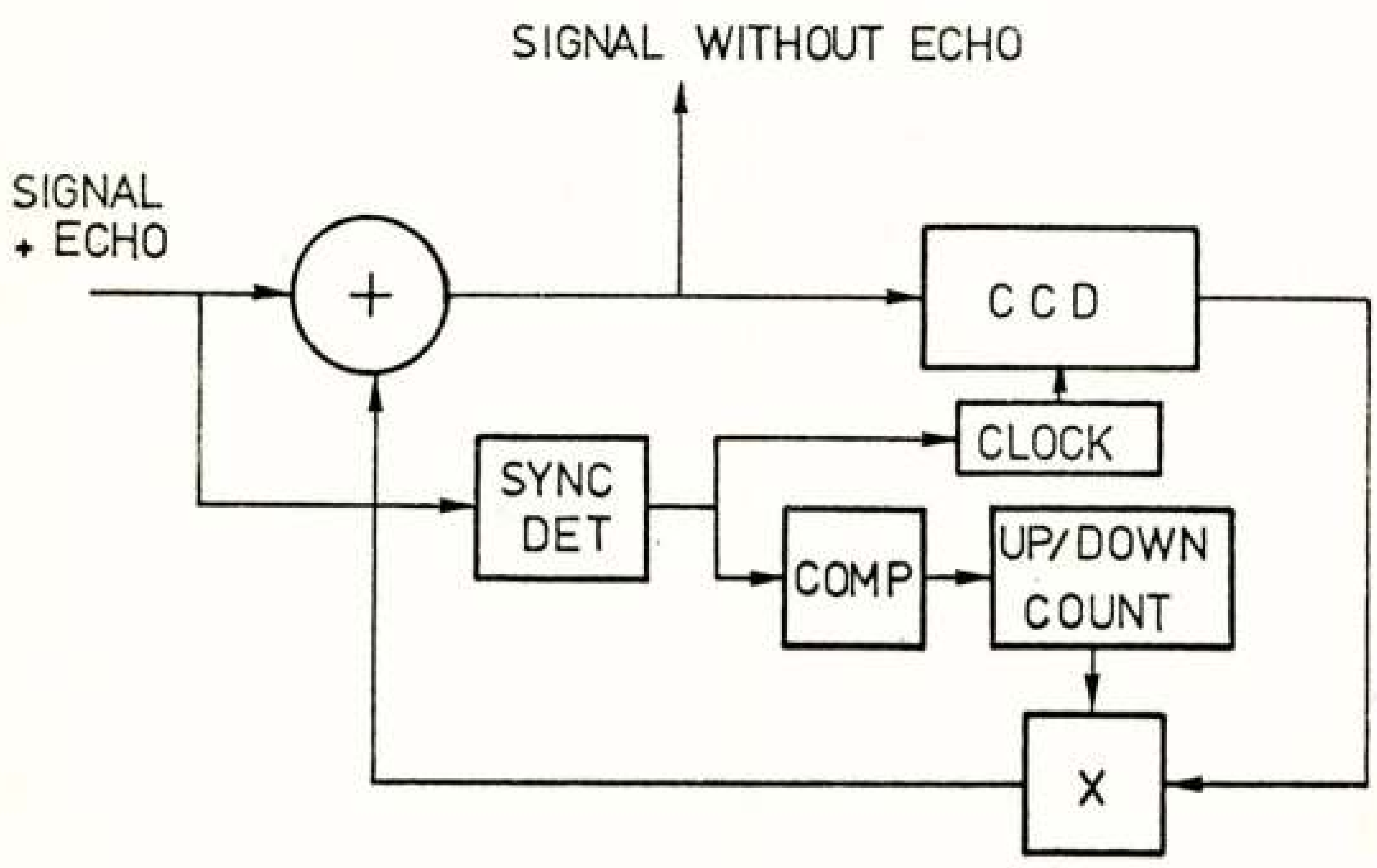


Fig. 2

Bloc-diagram of the echo-cancellation circuit.

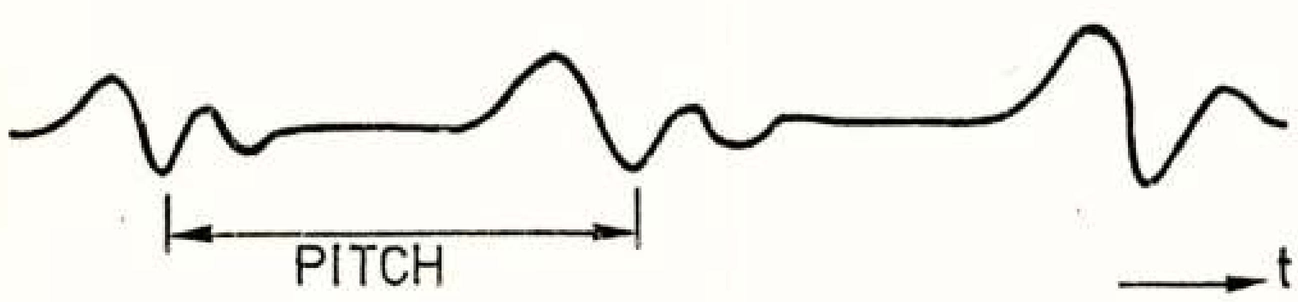


Fig. 5

Voice signal.

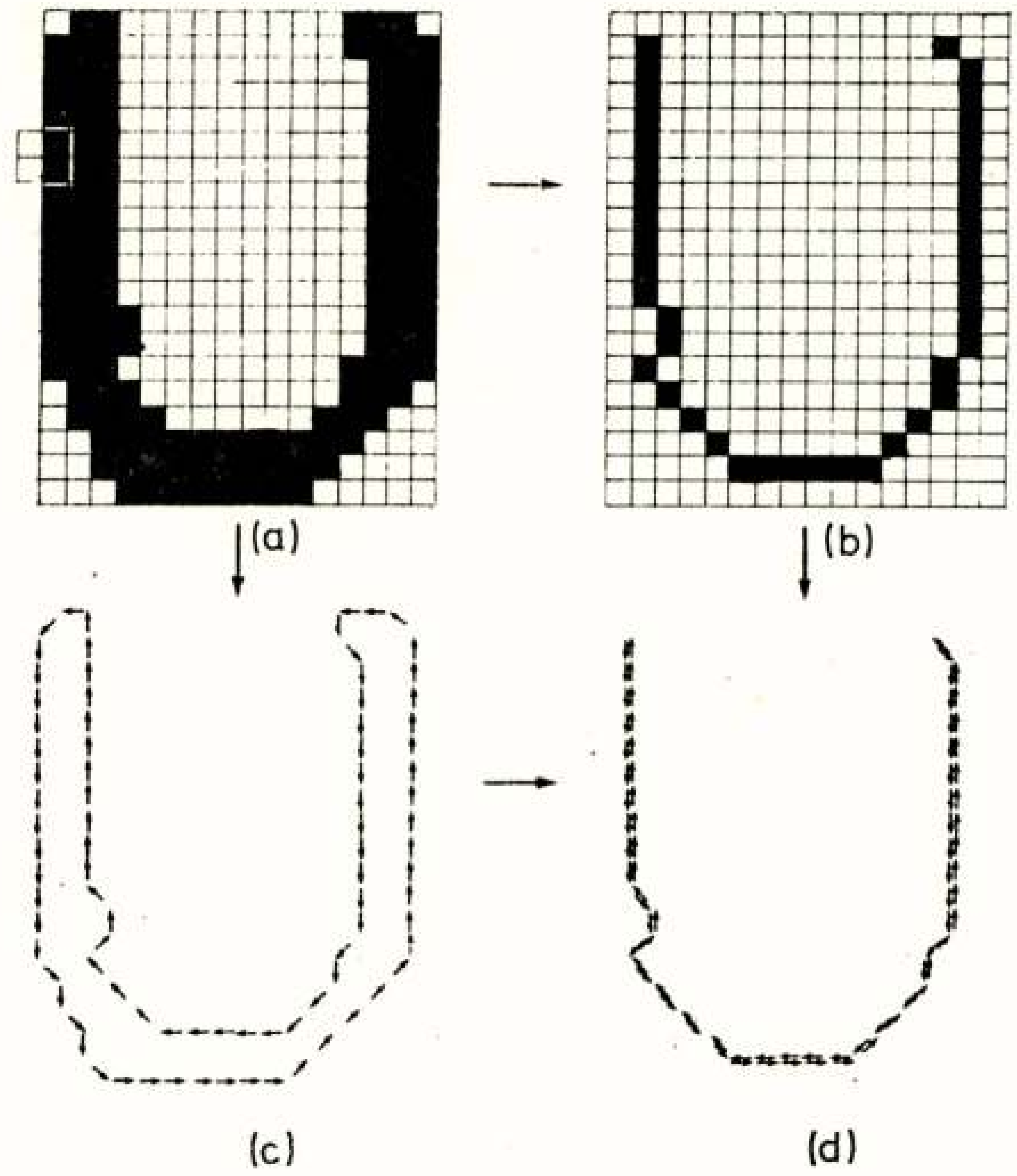


Fig. 3

a) Binary image of a U
b) Peeled character
c) String of tangent vectors before peeling
d) String of tangent vectors after peeling.

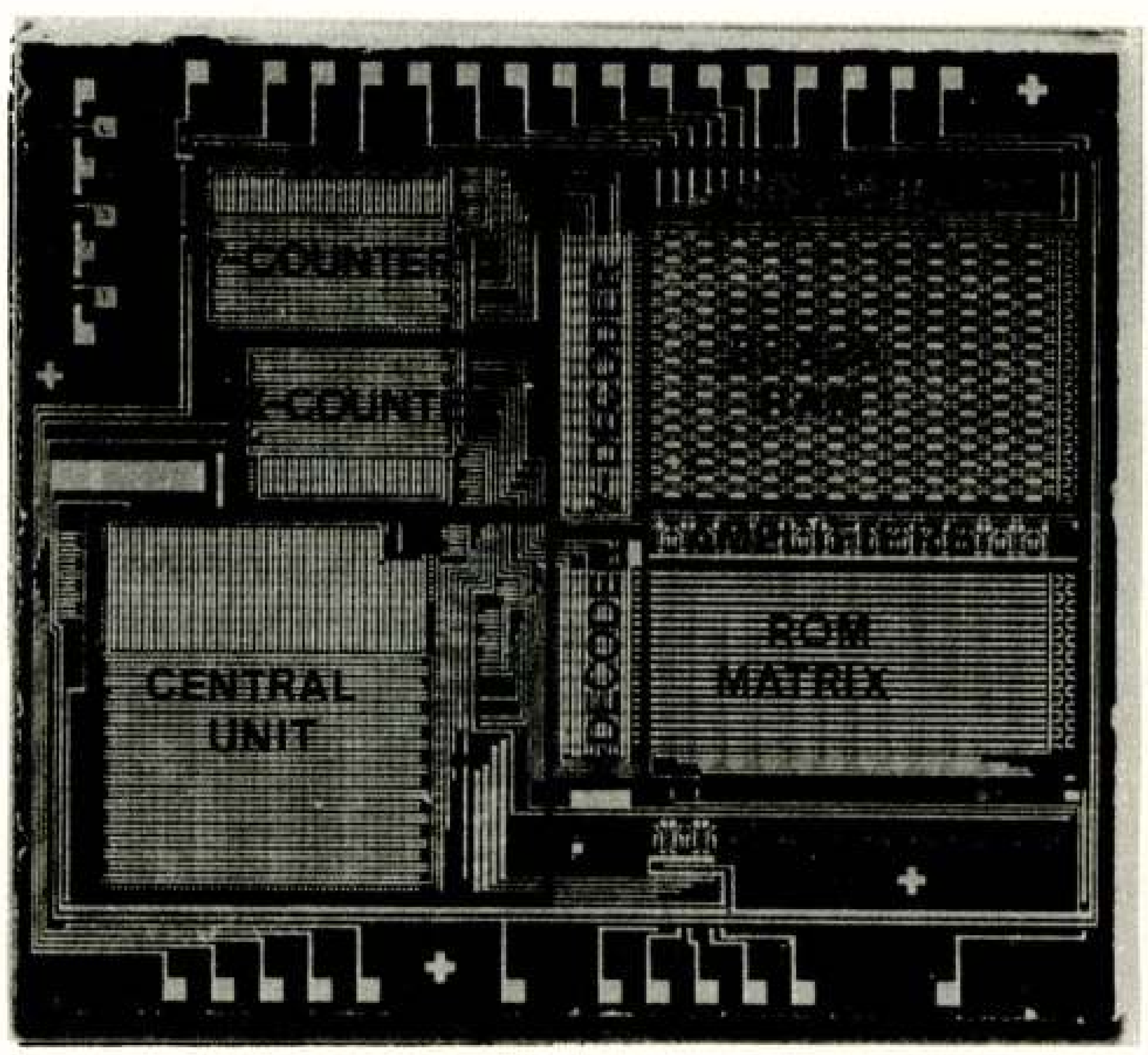


Fig. 4

Microphotograph of contour following circuit.

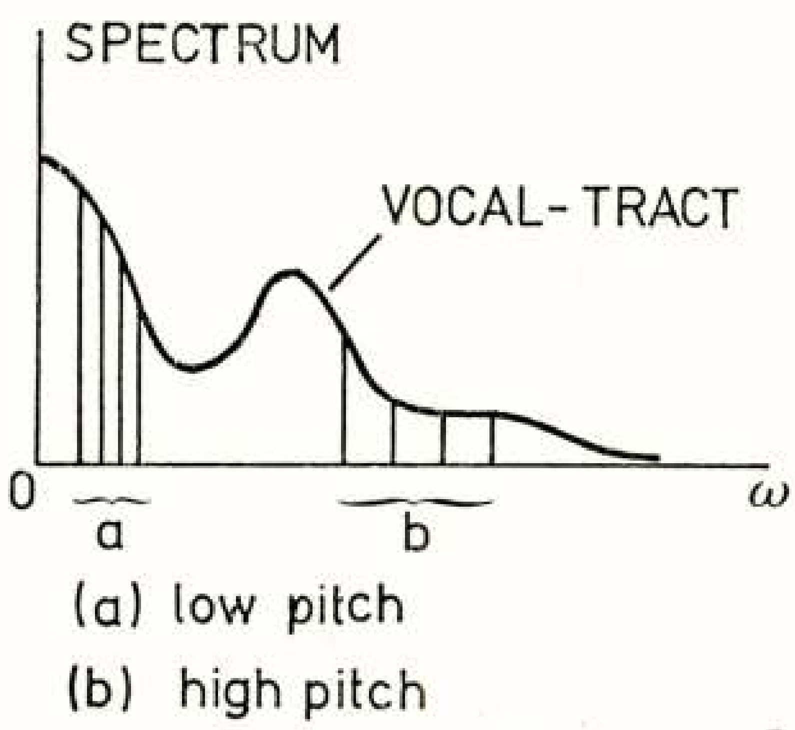


Fig. 6
Short time Spectrum of voiced signal.

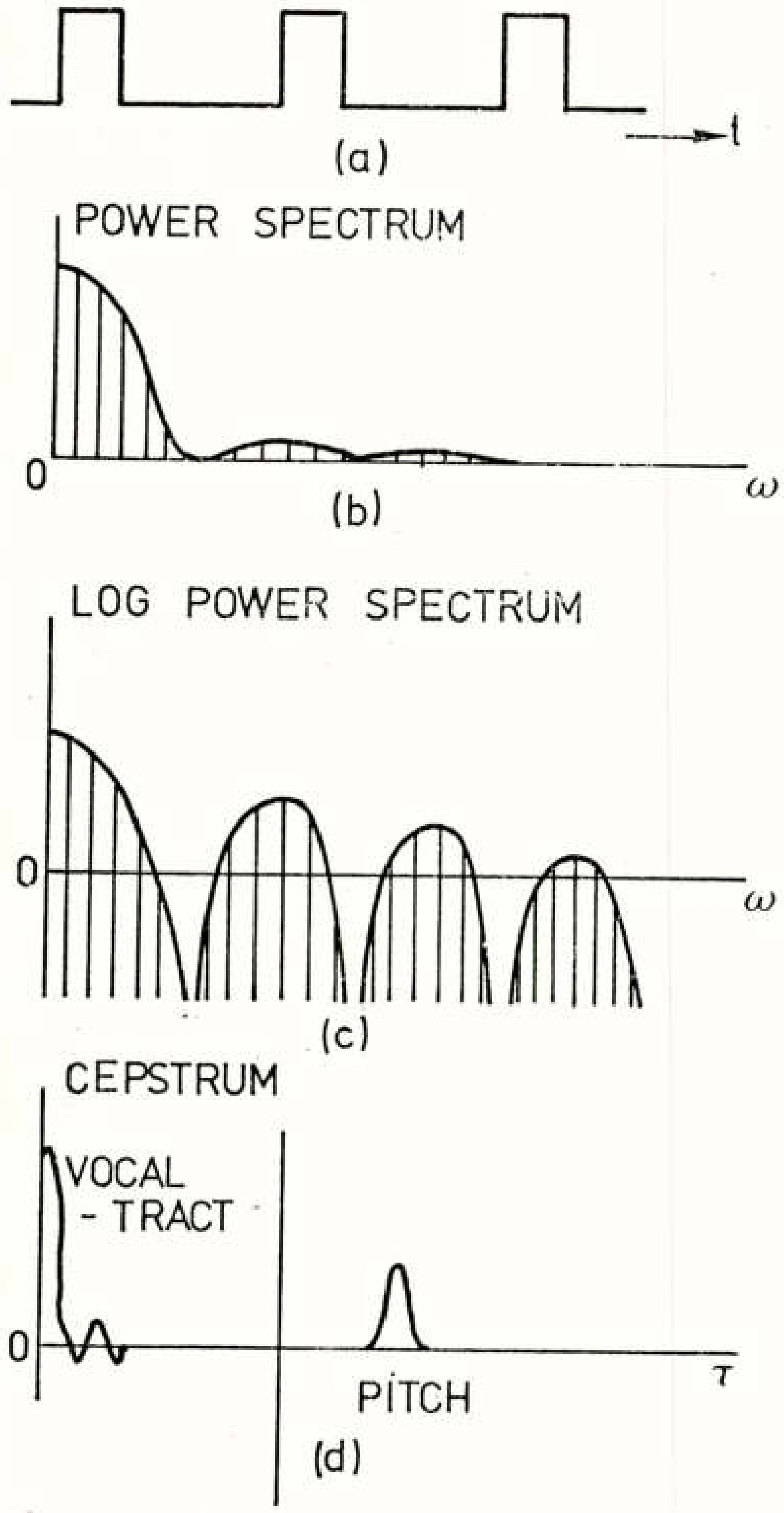


Fig. 10 Pitch determination by means of the Cepstrum
- a) Periodic square wave
- b) Power Spectrum
- c) Log. power Spectrum
- d) Cepstrum

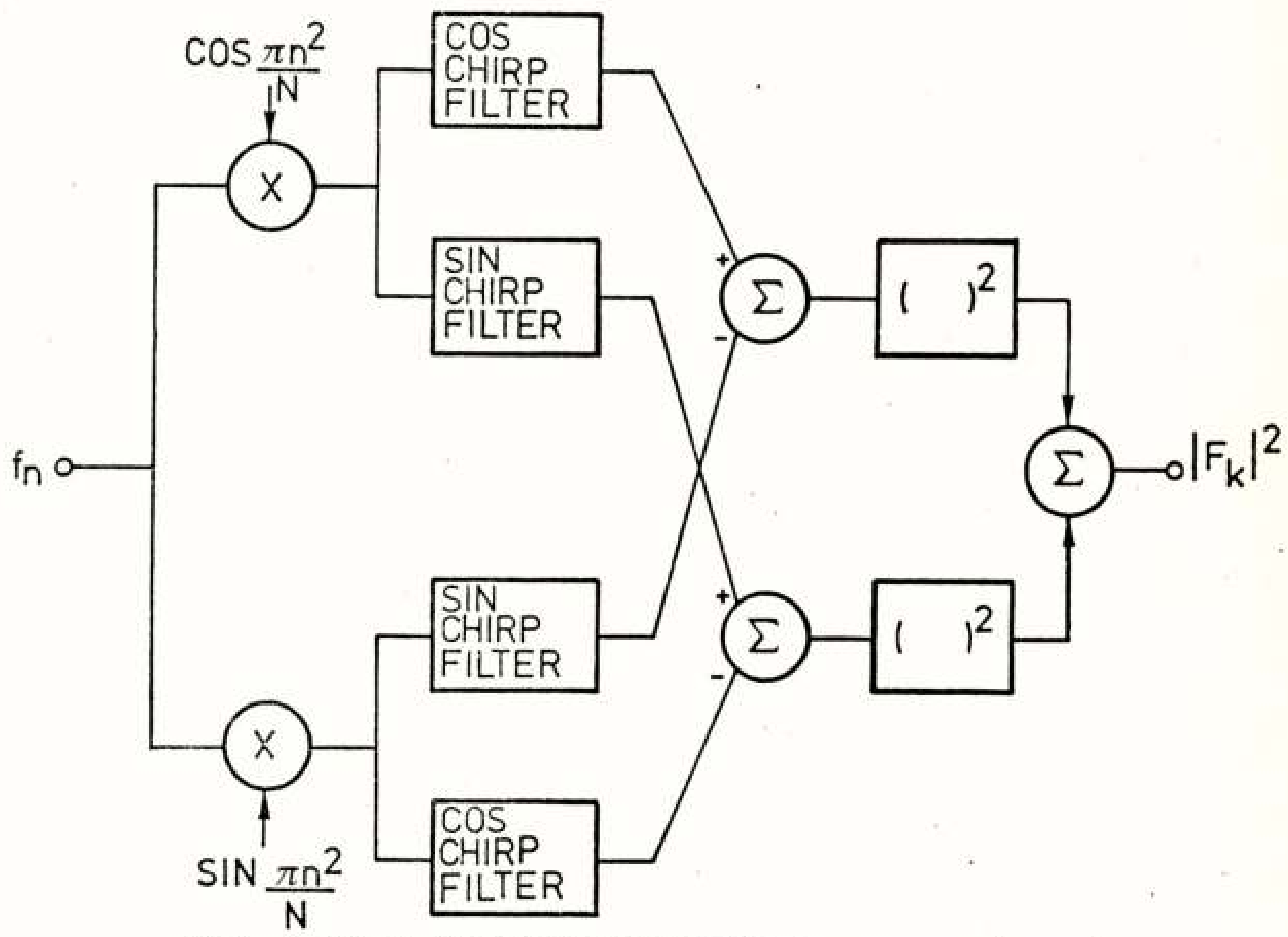


Fig. 9 Power Spectrum evaluationby means of quad chirped transversal filter.

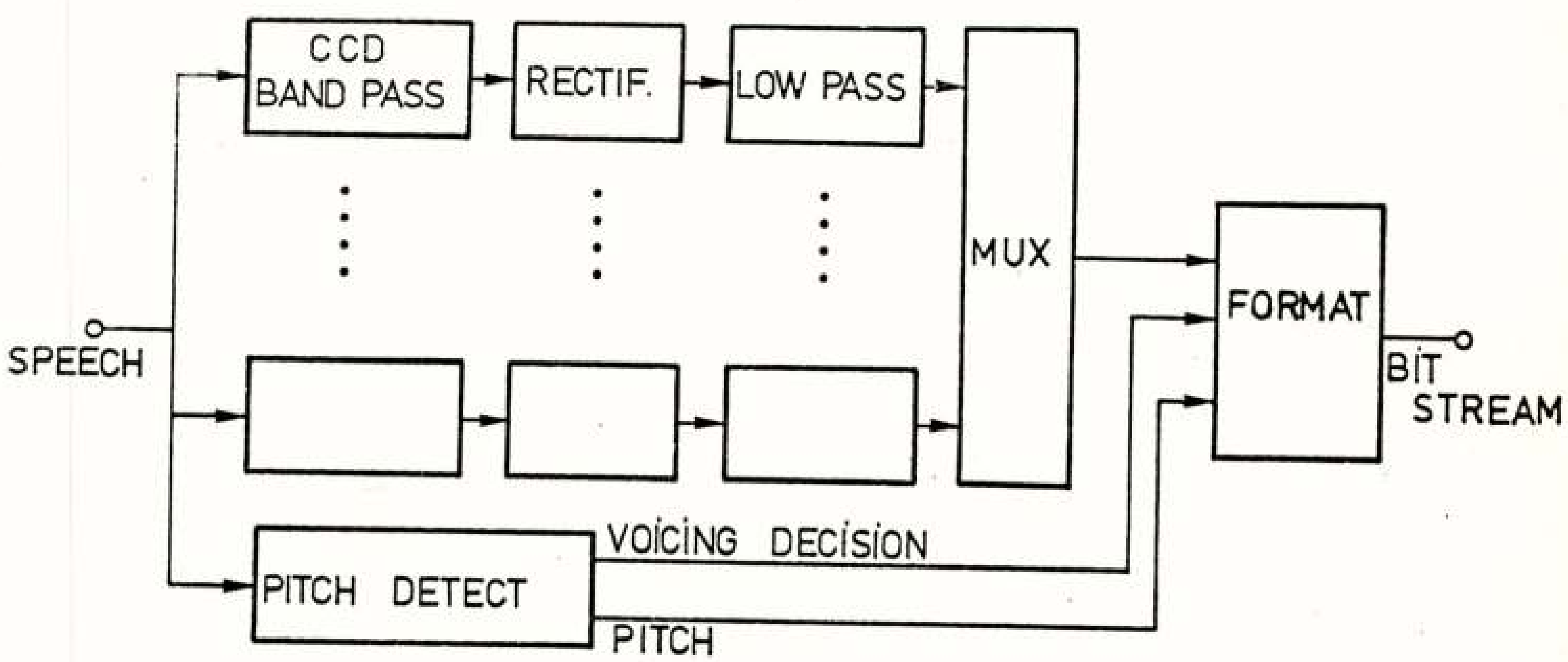


Fig. 7 Bloc-diagram of a Vocoder.

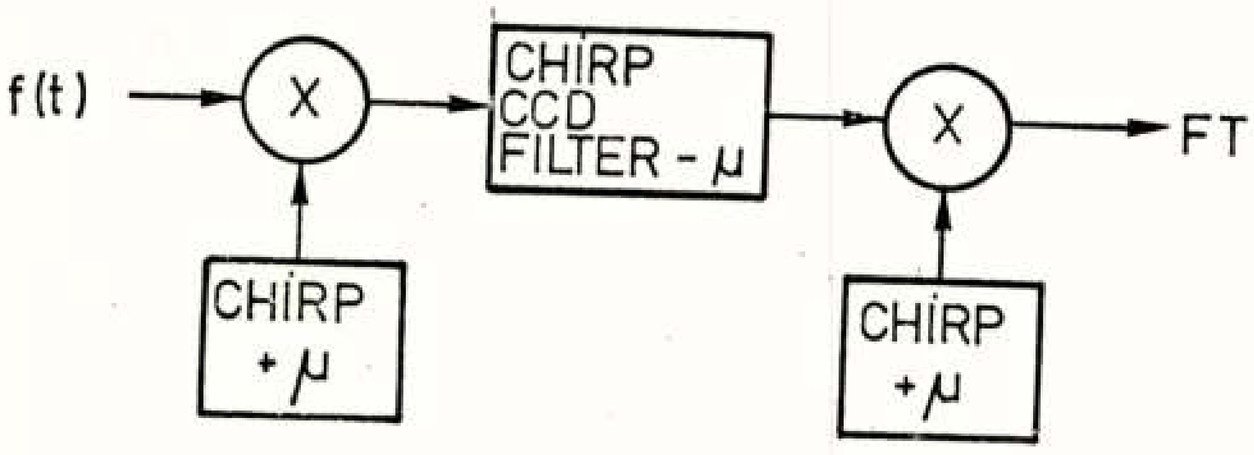


Fig. 8 The chirp Z Fourier Transform.

DESIGN AND APPLICATIONS OF ADAPTIVE GYRATORS

J.O. Voorman

Abstract

Gyrator principles - definition, electronic design and controllability - are explained. Filter applications as well as oscillator applications (ending up with the PAGYR IC) are surveyed with reference to the various gyrator properties exploited.

Introduction

In 1948 Tellegen presented his famous paper : "The Gyrator, a new electric network element" [1]. He introduced the gyrator as a passive electric two-port with equations

$$i_1 = +Gv_2, \quad i_2 = -Gv_1, \tag{1}$$

where G is the gyration conductance. The opposite signs in the two equations indicated something new: the gyrator is non-reciprocal.
The best-known passive implementations (in microwave isolators and circulators) were based on the Hall effect and on the Faraday effect. For low frequencies the artificial inductance of a capacitively loaded gyrator is an attractive proposition for simulating bulky and expensive coils. A satisfactory implementation was not found, however, until active parts were used for the gyrator construction. The first to be introduced was a triode gyrator (Wheeler 1948, Klein 1952), followed by a pentode gyrator (Sharpe 1957) and a first transistor gyrator (Ghausi and McCarthy 1963). It is due particularly to the rapid development of integrated circuits that practical gyrators have become feasible devices.

Construction principle of an electronic gyrator

A straightforward implementation of the gyrator equations (as two voltage-controlled current sources) is shown in fig. 1. The accuracy requirements, comparable to those for coils, necessitate the use of composite (artificial) transistors where a single transistor is drawn in fig. 1. Supply current circuitry completes the gyrator. An integrated version (TCA 580) is on the market [2, 3].

Signal amplitude detection on a gyrator-capacitor resonant circuit

Let us consider a "symmetric" resonant circuit (constituted by a gyrator with a capacitor connected across its secondary port, thus forming together an inductance, shunted by another capacitor of the same value). We apply a signal current of variable frequency (fig. 2).

Voltage v_1 shows a resonance character. The resonant frequency is

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{G}{C}. \tag{2}$$

So far there is nothing unusual.

However, unlike in the case of an LC resonant circuit, we can measure a second voltage (v_2), which shows a similar resonance character. If

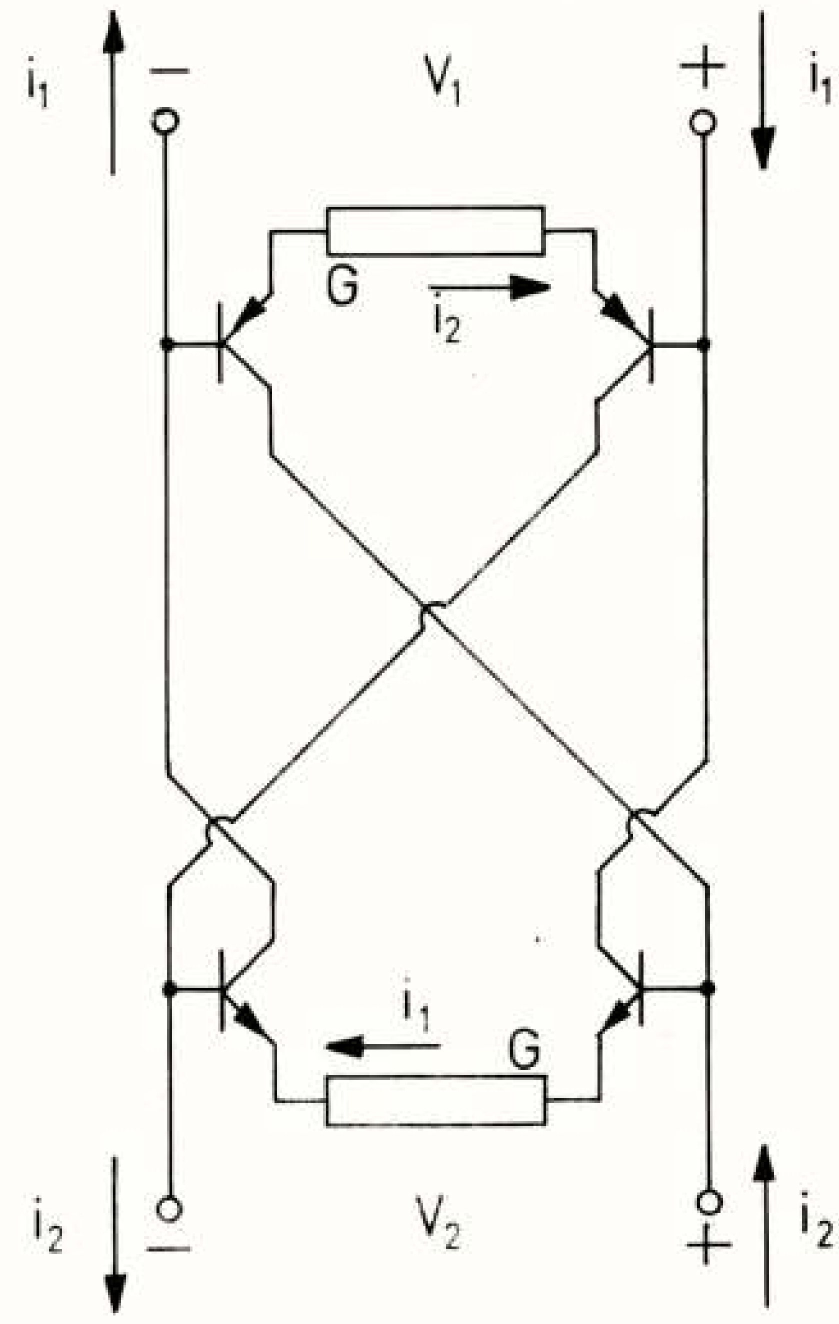


Fig. 1. Principle of the construction of an electronic gyrator from two voltage-controlled current sources ($i_1 = +Gv_2$, $i_2 = -Gv_1$).

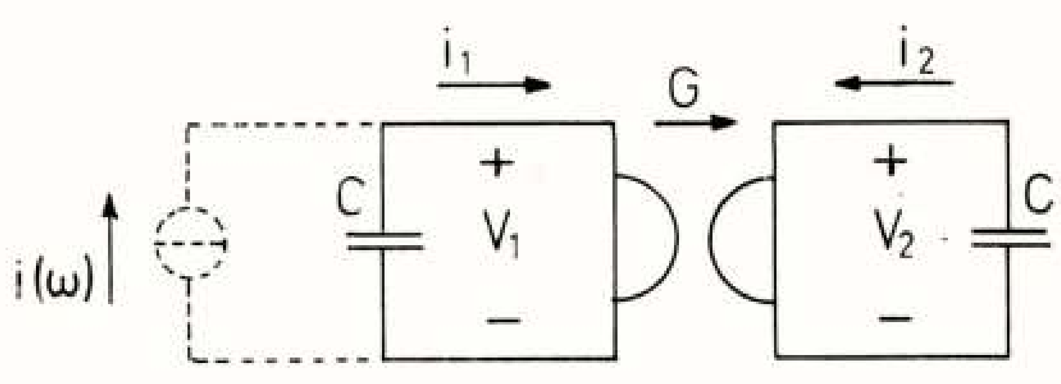


Fig. 2. A "symmetric" gyrator-capacitor resonance circuit.

$$v_1 = a \cos\omega t, \tag{3}$$

then

$$v_2 \approx a \sin\omega t. \tag{4}$$

The two voltages have equal amplitudes and a 90° phase difference. The electric charge is "toggling" between the two capacitors.

A similar relationship is found for the signal currents ($i_1 \approx b \sin\omega t$, $i_2 \approx -b \cos\omega t$). Therefore,

$$(i_1^2 + i_2^2)^{\frac{1}{2}} = b \tag{5}$$

is a yardstick for the signal current in the gyrator.
The above property can be used essentially in two ways :
- in filter applications to control the supply current in the gyrator (in proportion to the signal level), thus saving mean supply power, and
- the amplitude b can be stabilized to some reference value b_0 (if $b > b_0$ the resonant circuit is damped, if $b < b_0$ it is undamped) and an oscillator is obtained.

Filter applications

The first aim in designing electronic gyrators was

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to simulate inductance. Particularly important in this application is the lossles̲s̲n̲e̲s̲s̲ of the gyrator [4].

In other applications the non-reciprocity, or better the anti-reciprocity, plays a crucial role, for instance in quadrature filters. An example is a matched-filter receiver for FSK signals [5].

Variable gyrators (i.e. gyrators with a variable gyration conductance) can be employed in variable filters. From the basic gyrator construction in fig. 1 it is seen that two conductances have to be varied together. The above can be obtained with current multiplication based on the exponential characteristic of bipolar transistors [6].

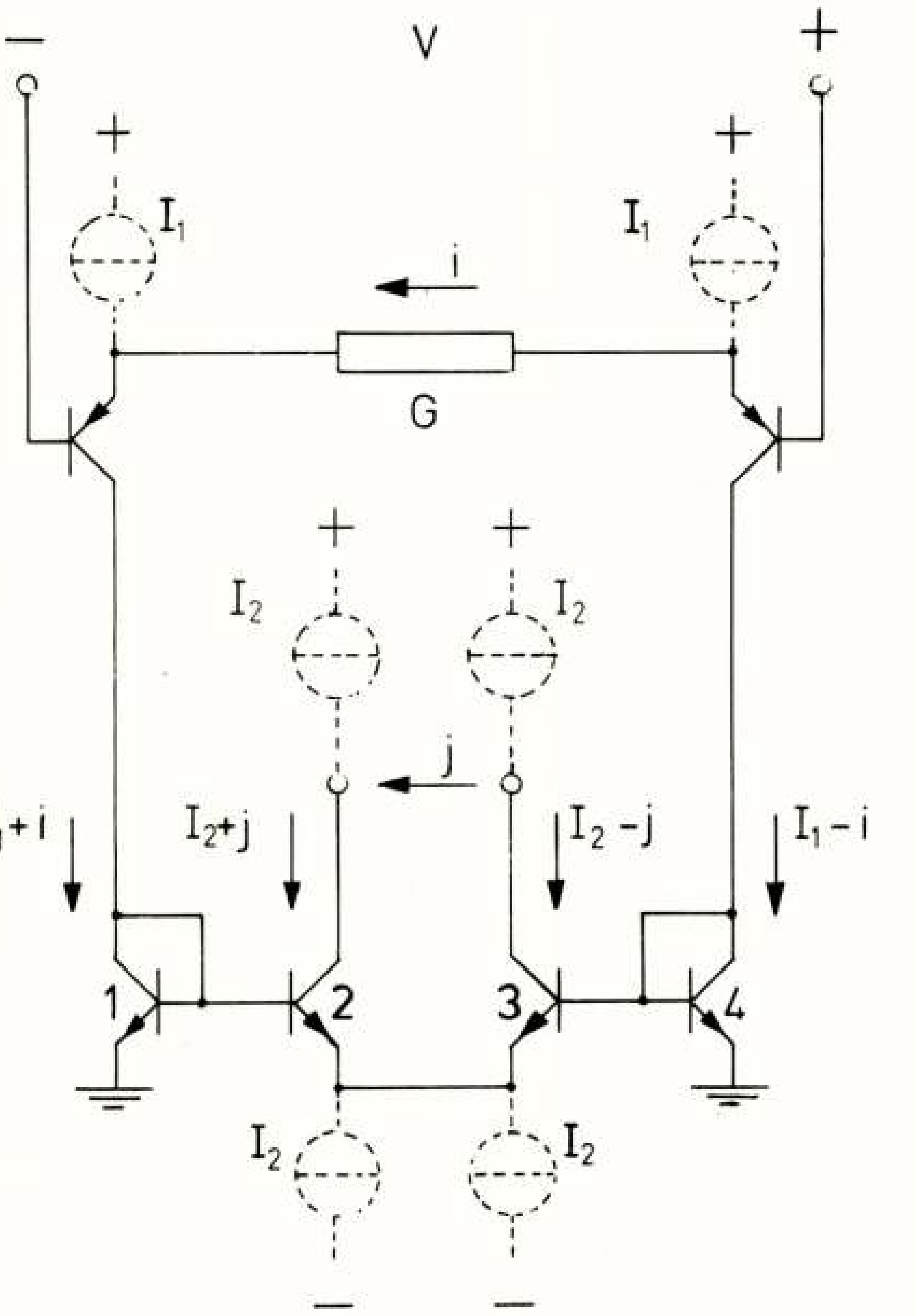


Fig. 3. Variable transconductance principle. Input voltage v causes a current i in conductance G. For the matched transistors 1, 2, 3 and 4 : $V_{BE1} - V_{BE2} + V_{BE3} - V_{BE4} = 0$ and hence $I_{C1}I_{C3} = I_{C2}I_{C4}$ or $I_1 j = I_2 i$. The transconductance j/v is GI_2/I_1, from which the ratio of the supply currents I_2/I_1 can be varied.

In fig. 3 the principle of a variable voltage-controlled current source is shown. Its transconductance is given by

$$\frac{j}{v} = G\,\frac{I_2}{I_1}\ . \qquad (6)$$

Two stages in anti-parallel (fig. 1) form a variable gyrator. The supply current ratio I_2/I_1 controls the gyration conductance. An accurate design, free from latch-up and stable with overflow, is shown in figures 4a and 4b.

Adaptive gyrator

An adaptive gyrator is variable and has squarers for signal amplitude detection (eq. 5). A squarer

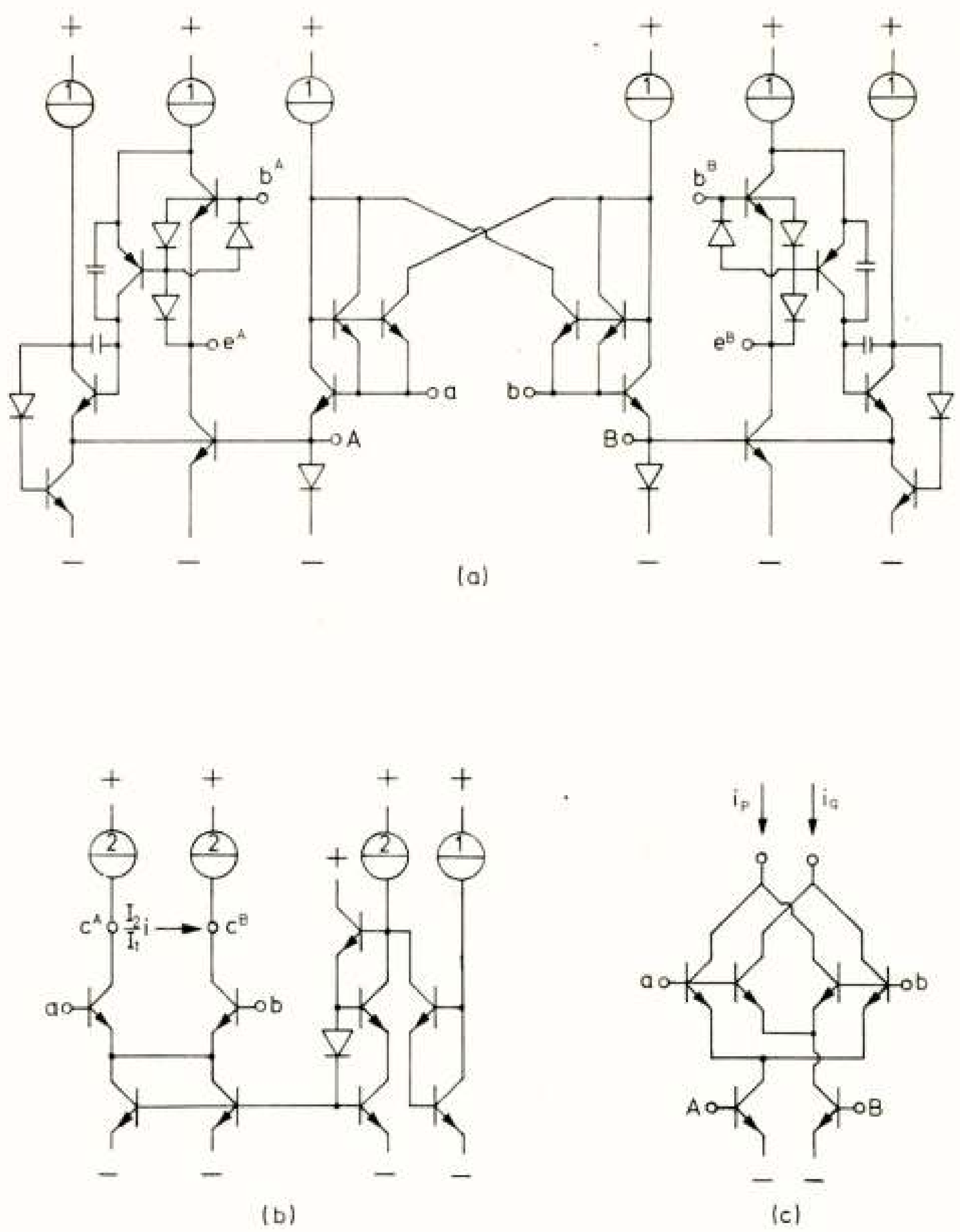


Fig. 4. Adaptive gyrator stage. An input voltage v (between b^A and b^B) causes a current i in a conductance G (to be connected between e^A and e^B). The output current iI_2/I_1 (compare with fig. 3) is taken from c^A and c^B. In fig. c a squarer (see eq. 5) is shown. Two of these stages connected in anti-parallel form an adaptive gyrator.

is shown in fig. 4c. Its output current is given by

$$i_p - i_q = 2\,\frac{i^2}{I_1}\ , \qquad (7)$$

where i is the signal current induced in the gyration conductance G (to be connected between e^A and e^B).

The adaptive gyrator chip (fig. 5) contains integrated gyration conductances. The supply current ratio I_2/I_1 is derived from the ratio of an external conductance G_e and a likewise integrated conductance G_i. Thus, the effective gyration conductance

$$G_{eff} = \frac{G}{G_i}\,G_e \qquad (8)$$

contains the accurate (fixed) ratio G/G_i of matched monolithic conductances.

Gyrator oscillator

The detection of the amplitude b of the signal current in the gryator is described in eq. 5. A principle of amplitude stabilization is illustrated in fig. 6. Two controlled signal current sources damp or undamp the circuit, depending on the sign of ε.

The descriptive equations are

$$C\frac{dv_1}{dt} + \varepsilon G v_1 + \frac{I_2}{I_1} G v_2 = 0,$$
$$C\frac{dv_2}{dt} + \varepsilon G v_2 - \frac{I_2}{I_1} G v_1 = 0. \qquad (9)$$

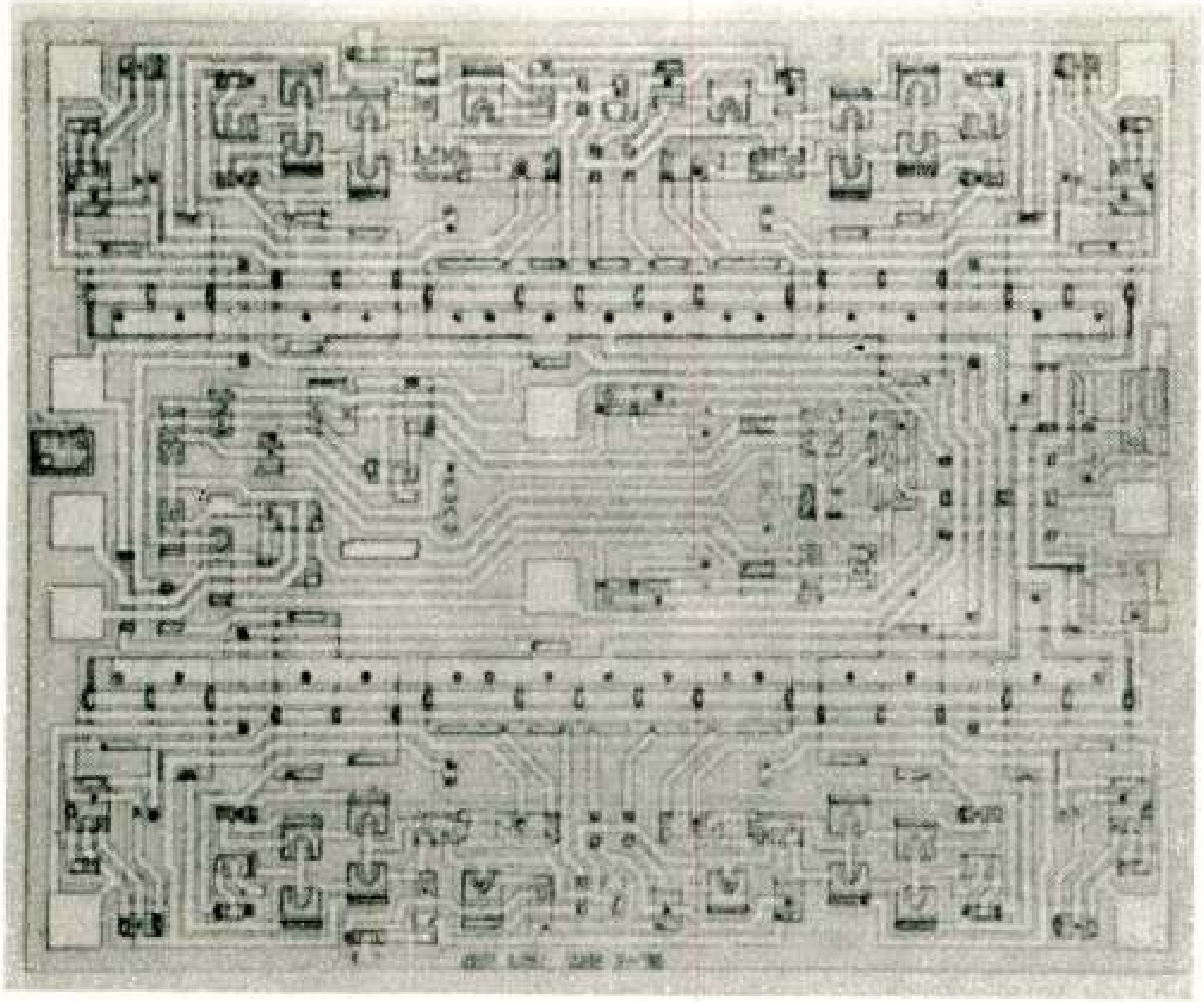


Fig. 5. Experimental adaptive gyrator chip (2x3 mm^2). Its gyration conductance is controlled by a single external resistor. The signal amplitude detection can be used either for supply current control (in filters) or for signal amplitude stabilization (oscillators).

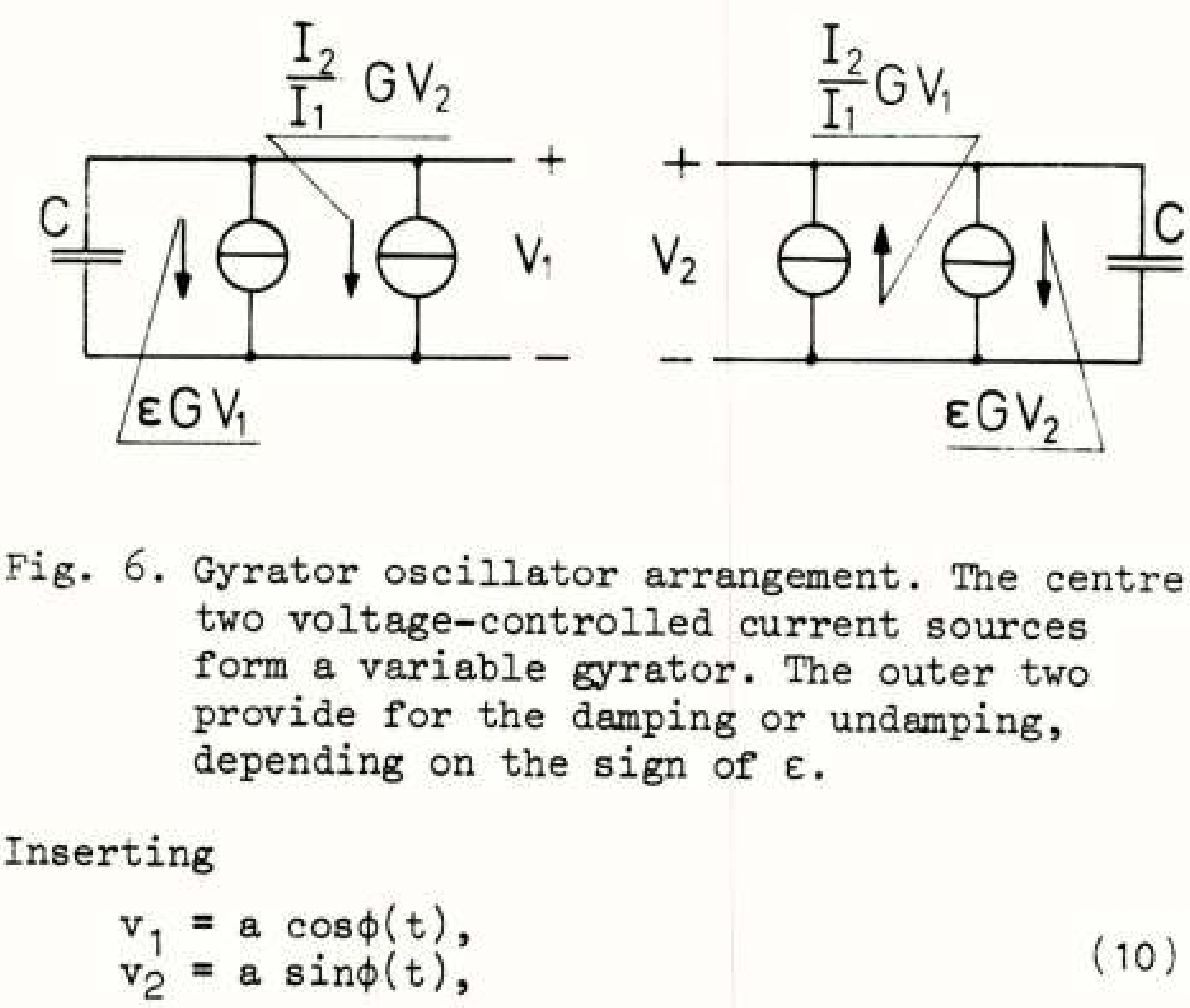


Fig. 6. Gyrator oscillator arrangement. The centre two voltage-controlled current sources form a variable gyrator. The outer two provide for the damping or undamping, depending on the sign of ε.

Inserting

$$v_1 = a \cos\phi(t), \quad v_2 = a \sin\phi(t), \qquad (10)$$

the variables can be separated (which is not possible in the case of a Van der Pol oscillator) [7]. The result is

$$\frac{da}{dt} + \varepsilon \frac{G}{C} a = 0, \qquad (11)$$

$$\frac{d\phi}{dt} = \frac{G}{C} \frac{I_2}{I_1}. \qquad (12)$$

The oscillator gives two output signals in quadrature (eq. 10). The amplitude is stabilized at a value a_o, where $\varepsilon(a_o)=0$ and $(a-a_o)\varepsilon(a) > 0$ for $a \neq a_o$ (eq. 11). The instantaneous frequency of the signal is directly controlled by the value of I_2 (eq. 12). The arrangement is an ideal frequency modulator [8].

Gyrator oscillator applications

The gyrator oscillator is ideally suited for low frequency FM, PM and FSK transmitters. An example is an FSK transmitter. Its bandpass filter can be avoided by applying a combination of trapezoidal frequency modulation and some percents of amplitude modulation [5].

In phase and frequency locked loops the clean sine-wave (no locking on harmonics and subharmonics) and the availability of the quadrature signal can be of advantage. An example of the above is the PAGYR.

PAGYR

The PAger GYRator circuit [9] is the selective part of a tone encoder/decoder intended for use in selective calling in mobile radio. Call codes are dealt with on a digit by digit (tone by tone) basis.

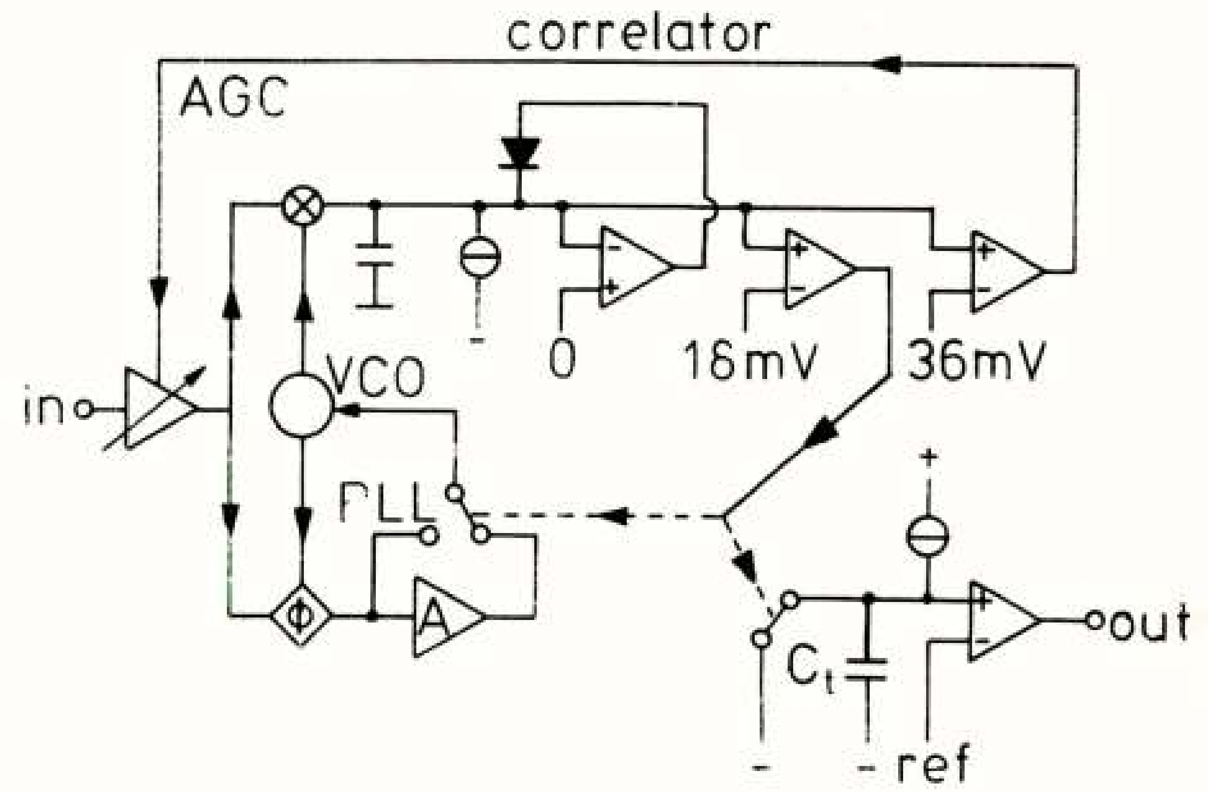


Fig. 7. Block diagram of the PAGYR.

The block diagram of the PAGYR (fig. 7) shows a gyrator Voltage-Controlled Oscillator (VCO) with two quadrature outputs in a Phase-Locked Loop (PLL). The oscillator is switched from frequency to frequency by switching a resistor array. The correlator detects whether there is an input signal or not and it controls the switching of the loop gain of the VCO (for fast acquisition). If a tone is found present during a certain time the output goes "high". The switching from tone to tone, from encoding to decoding, relaying etc. is controlled by a second integrated circuit.

The PAGYR is integrated in a standard bipolar process. The chip size is 2x4.2 mm^2. It contains 360 components (fig. 8). Relevant circuit parts

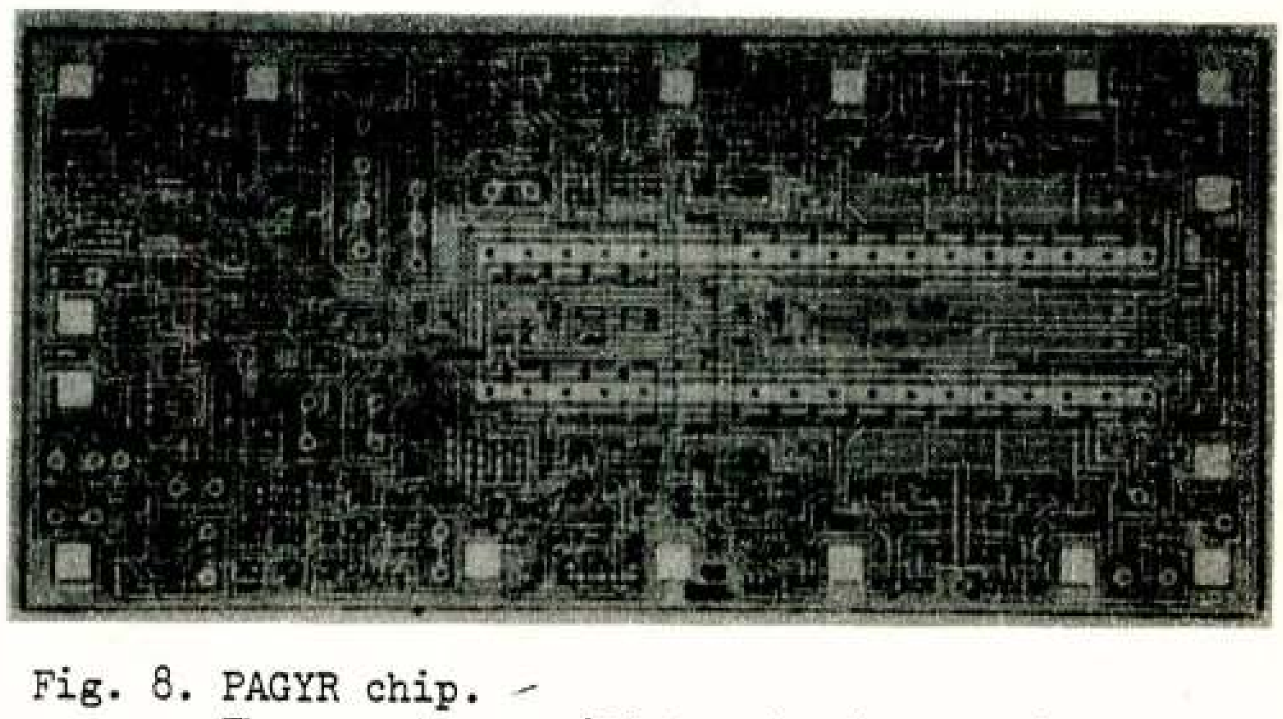


Fig. 8. PAGYR chip.
The gyrator oscillator is in the right hand part. The circuit is integrated in a standard bipolar process and measures 2x4.2 mm^2.

are compensated for base current and Early effect. Component positioning on the chip is such that linear gradients in transistor and resistor properties have no influence on the circuit behaviour. Some further data are

supply voltage : 3 - 10 V,
power consumption : 1 mW (3V),
frequency range : 50 - 5000 Hz,
(linearly controlled)
capture range (2 - 20 %),
(either proportional to or independent of oscillator frequency)
AGC range : 40 dB.

Conclusion

A survey of the properties and applications of adaptive gyrators reveals their attractiveness as new components for integrated selectivity. Filter applications (inductance simulation, quadrature filters, variable filters) and oscillator applications (ideal frequency modulator, FSK transmitter, PAGYR) are distinguished. The PAGYR IC proves the feasibility in production.

References

(1) B.D.H. Tellegen (1948)
"The Gyrator, a new electric network element"
Philips Res. Reports 3, 81-101.

(2) J.O. Voorman and A. Biesheuvel (1972)
"An electronic gyrator"
IEEE J. of Solid-State Circuits SC-7, 469-474.

(3) Philips, Electronic Components and Materials
- Data handbook (1976)
  Semiconductors and Integrated Circuits
  Professional analogue IC's
- "The TCA 580 integrated gyrator"
  Electronic applications bulletin 34 (1977)
  109-122, 148-161.

(4) H.J. Orchard (1966)
"Inductorless filters"
Electronics Letters 2, 224-225.

(5) J.O. Voorman (1977)
"The gyrator as a monolithic circuit in electronic systems"
Thesis, University of Nijmegen.

(6) B. Gilbert (1968)
"A new wide-band amplifier technique"
IEEE J. of Solid-State Circuits SC-3, 353-365.

(7) N. Minorsky (1947)
"Introduction to non-linear mechanics"
Ann Arbor, Edwards.

(8) J.O. Voorman (1974)
"Ideal frequency modulator"
Electronics Letters 10, 387-388.

(9) J.O. Voorman and A. Wijker (1978)
"PAGYR, a new component for selective calling"
Philips Telecommunication Review 36, 31-40.

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REVIEW OF THE EVOLUTION OF TELETEXT AND VIEWDATA.

Gerald Offley Crowther

1. Introduction

The words Teletext and Viewdata have created a major impact on the electronics industry involving most of the major branches: Broadcasting, Telecommunications, the Television and Data Handling industries. The detailed interests of each individual industry are clearly different and there is now a danger that the initial benefits, low cost standard communication systems, may be lost in the conflict of different aims.

It is perhaps useful to review the aims and reasons which led to the adoption of the present U.K. Teletext and Viewdata systems.

The two systems have always been regarded as complementary. Teletext provides a natural method of providing rapidly changing information to many users. Viewdata, on the other hand, supplies individual data from a wide data base. As a consequence, it has been regarded as fundamental that the two systems should be economically compatible.

The prime aim for both systems has been to bring data handling systems into the home as part of the domestic colour T.V. set, thus creating a new and potentially large market. It was recognised from the outset that the two systems would also be of great interest to the professional areas (specifically Viewdata) where the final requirements may be significantly different to those of the domestic market.

In the design specifications of both systems considerable attention has been paid to minimising the additional cost onto the domestic colour T.V. set in the initial stages. At the same time redundancy has been incorporated to allow significant enhancement of the user facilities as advances in semiconductor technology permit and the needs arise without imposing cost penalties on the basic decoder. The above feature has been achieved in such a way that the present LSI decoder systems will continue to function correctly by rejecting signals intended for more enhanced decoders.

A number of doubts and uncertainties have been expressed as to the suitability of the present U.K. specifications for Europe, U.S.A. and other locations.

The comments centre around four main topics:-

1. The data rate of Teletext,
2. The fixed relationship between transmitted data on a T.V. line and the displayed row of Teletext,
3. The extension for European and non-Latin languages (both systems),
4. The display control facilities (both systems).

2. Choice of Data Bit Rate in Teletext

The choice of data bit rate is a compromise between the bandwidth of the system and the desire to maximise the data transmitted within the given bandwidth.

The present data clock rate of 6.9375MHz was based on an extensive field trial on System I (1 & 2) in the U.K. and System B (3) with data clock rates ranging from 4.5MHz to the present 6.935MHz. The error rates over the whole range were insignificantly different.

Subsequent experience in the U.K. has proved the choice to be the correct one and this is being confirmed in some European countries.

Significant problems have, however, arisen in countries with mountainous regions due to short echoes insufficient to disturb the T.V. picture. It has been shown by RAI in Italy (4) that a significant improvement can be achieved by the use of biphase bit coding rather than the present NRZ system but at the severe penalty of halving the data rate for the same data clock rate. The improvement is associated with the better clock synchronisation and smaller bandwidth of the data signal.

A judgement has now to be made whether to:-

1. adopt the biphase system and accept the reduction in data rate by a factor of two,
2. adopt biphase system only where the terrain forces its adoption,
3. improve the present NRZ receiver decoders to cope with the large echoes.

Option 3 has major attractions since the main user criticism of Teletext is the waiting time.

It would also appear that the margin of improvement required could be achieved by the natural advances in T.V. set design resulting from LSI technologies coupled with improvements in the transmission system (particularly the introduction of data regenerators).

The features made possible by LSI technology are accurate digital tuning, surface wave i.f. filters, synchronous detection and, in the future, echo cancellation.

The major improvement will undoubtedly come in better techniques for data recovery in the Teletext decoder. The present decoders employing peak to peak detection are particularly susceptible to echoes. There is good reason to believe that better techniques will be available in the foreseeable future.

Option 2 is a possible solution and LSI receiver decoders could be designed to automatically switch to the appropriate system with minimum on costs.

In conclusion, it must be stated that neither solution is suitable for NTSC systems. Compatible systems can be designed readily which permit the use of the present LSI decoders with minor modifications. This can be achieved either by reducing the clock rate by a factor of two and only transmit half a row of data per T.V. line or by reducing the number of characters displayed per row from 40 to 32 and, therefore, reduce the clock rate. The former solution is to be preferred as it gives more optimal display format.

3. The Direct Relationship Between The Data Inserted on a T.V. Line and a Displayed Data Row in Teletext

At the outset it has to be recognised that Teletext, unlike Viewdata, is a non-interactive system. The transmission and decoder concepts have to be designed to give the user the appearance of an interactive system.

There are two instances where the fixed relationship between the transmitted data and display data on a T.V. line is of importance. The first when the user requests a new page and, secondly, when errors occur in the transmission.

To cover the first aspect all present LSI decoders display on screen every page header. Since the page number is always transmitted in the same location it will appear on screen as a continually changing or rolling display. It has been arranged that the page number rolls from the instant the new page is requested until its acquisition. The user is given immediate feedback, the system is functioning correctly even though the page requested is not being transmitted. Other variants on the facility are clearly possible but they can only be achieved economically if the one-to-one relationship exists.

More important, is to examine the effects of errors in a transmission. If errors occur either detected or undetected, the only possible action is to wait for a repeat transmission. Furthermore, since errors are likely to be caused by noise, probably aided by other distortion phenomena (reflections, asymetric distortions in equipment and co-channel interference); it is probable that the next reception of the required text will contain errors in new locations. Advantage can be taken of this fact if the coding system is well chosen. It can be arranged that an integration of correct text automatically takes place by the use of simple parity checks over two or three receptions of the wanted data. For this to be achieved it is vital that the page selection and the page formatting information is protected against disturbance. Hamming codes for the protection and correction of the address data are employed.

At first sight it would appear that the integration can be achieved without the strict relationship with considerable advantage in the display facilities.

In a non-synchronous system the presence of page formatting information has to be marked by a flag. The flag to be recognised has to be of the same form as the data and is, therefore, just as corruptible. If the flag is missed for any reason, the decoder must interpret the following information as data which could be the start of an unrelated page. Thus, rather than obtaining the desired integration of correct data, the reverse may well occur.

In the U.K. synchronous system the page formatting data always occurs at the start of a T.V. line and, in essence, the line sync pulses act as the flag. The normal flywheel techniques give complete protection to this method of flagging.

In conclusion, it is worth mentioning that conventional methods of protecting serial data such as BCC or CRC are not as effective as the combination of parity and Hamming protection.

4. Other Languages

It is recognised that the present Viewdata and Teletext proposals do not cater for the European and non-Latin languages. There is, however, redundancy in both systems to cater economically for both these requirements.

In both the systems the primary display medium is a conventionally scanned picture tube. This dictates that all characters have to be stored within the decoder character generator in the form in which they will ultimately be displayed.

To minimise the cost of the decoder it is essential to avoid code changing within the decoder and it is, therefore, necessary to transmit a simple seven bit code representing every character displayed. The use of the National usage codes of ISO646 can be exploited to achieve these aims. Normally, within a country a single language will be employed and each page may then be prefaced by a code representing the character set or language to be employed. The advantage of the proposal is that it simplifies the transmission by avoiding 'escape' sequences and retains the one to one relationship discussed earlier for Teletext.

In Viewdata the proposal is readily implemented by a single three character 'escape' sequence as defined in ISO2022.

For Teletext, use is made of spare codes built into the present specification. These include three control bits (C_{12}, C_{13} and C_{14}) and Rows 24 to 31 which present decoders must reject. It is permissible to raise one or more of these spare rows to the status of a page header or Row 0 with additional control bits with special meaning. One combination, for instance, would define the character set to be employed. A typical multilanguage transmission would then be as follows:-

Row 0	Page n	
Row 1	Character data	
.	. .	Page n recognised by
.	. .	present and future
.	. .	decoders (normal
Row 23	Character data	character set)
Row 0	Page 15 15	
Row 31	Page m language x	
Row 1	Character data	
.	. .	Page m and (m + 1)
.	. .	recognised by future
.	. .	decoders only
Row 23	Character data	
Row 31	Page (m + 1) language z	
etc.		

Existing decoders must not receive data initiated by the secondary page header (Row 31). Thus, Row 0 Page 15 15 is used as a terminator. This is a page which cannot be selected on any decoder but can be transmitted, and in common with all row 0's terminates the previous page. The page code 15 15 has already been used for this purpose in the U.K.

The techniques described above can be readily extended to give several languages on a single displayed page.

Before a scheme, as described above, can be imple-

mented, an agreement will have to be reached on how many additional characters will be permanently stored in ROM in the decoder character generator. It would be unreasonable to expect every symbol likely to be required to be permanently stored in every decoder. To cover the situation it has been proposed by the BBC (5) that the first part of the transmission should contain 10 X 6 dot pattern for a new character set which would be stored in a RAM but employed as a ROM within the decoder character generator. The techniques described above would enable the transmission of a full 96 character set in both Viewdata and Teletext. Furthermore, the proposal is a logical extension to the concept of the National usage codes.

To conclude, it is worth pointing out that the above technique can be employed to achieve enhanced graphics by joining together adjacent character blocks to form a single large block.

5. The Display Control Facilities

The display control facilities (colour of alphanumerics, flash, etc.) in the present systems are transmitted and stored in the decoder as part of the text. On the display these control characters are normally displayed as spaces. In most pages of text this is not a severe limitation, but it can be undesirable in certain displays employing the graphics capabilities of the system. The objectionable black space between a colour change can be avoided by employing the 'graphics hold' facility. In this case, the previously displayed graphics symbol is repeated in shape and colour at the location of the control character.

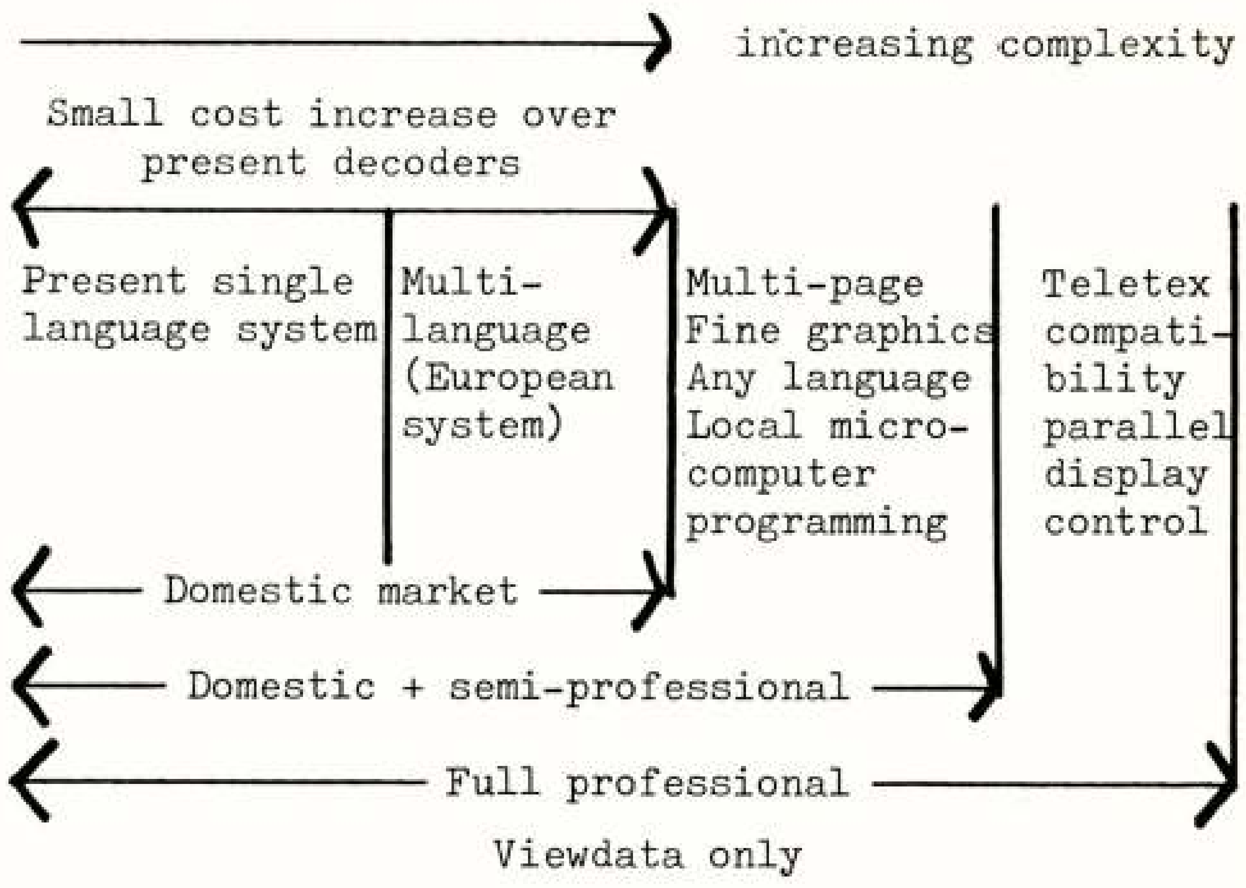
It has been proposed that a further enhancement of the system could be achieved if all the control characters could apply instantaneously to all display locations. The consequence of the proposal is that the memory size and, therefore, the cost of the decoder increases significantly but also the synchronous system for Teletext can no longer be employed. The proposal could, however, be implemented in Viewdata as an enhancement using the two character 'escape' sequences.

Before implementing parallel control characters, it is worth asking whether the necessary substantial and inefficiently employed memory could not be better employed for other features. As an example, a multipage memory would be of great benefit in both Viewdata and Teletext but would be prohibitively expensive with parallel display coding.

6. Conclusion

It has been demonstrated how the present U.K. systems can be enhanced to meet European and World requirements. It can be achieved with a minimum cost in the decoders and retaining the robustness of the present Teletext transmissions. The following table summarises the potential of the present Teletext and Viewdata.

The system has been designed for upwards compatibility.



References

(1). "Ceefax: Uhf Field Trials", By D.W. Stebbings, B.B.C. Research, April 1975.

(2). "An Assessment of Teletext Data Transmission over the Uhf Television Network", By L.A. Sherry, Teletext Transmission Working Group Note 10, I.B.A.

(3). "Teletext Field Tests in Bavaria April 16th to 24th 1975", August 1976, Published By the B.B.C., I.B.A. and I.R.T.

(4). "Technical Problems For Introduction In Italy Of A "Teletext" Service", By M. Cominetti, P. D'Amato, R.A.I., Turin, Italy.

(5). "Alphabets for Ceefax", B.B.C. Engineering, December 1977.

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TRENDS IN OPTICAL COMMUNICATION SYSTEMS

K. Mouthaan

Introduction

Less than a decade of research and development has taken glass-fiber optical communication systems from first experiments in the laboratory to complete trial systems already installed in the field and carrying regular telecommunication traffic now. A wide range of new technologies has had to be developed. Challenges in circuit design have emerged as well. Systems are being evaluated for use in the public telecommunications network as well as for use in other communications applications. New systems configurations are being conceived. At the same time, new options for systems of still higher performance appear on the horizon.

Advances in technology

The great strides that have been made in technology for glass-fiber optical transmission systems are exemplified by present-day availability of

- graded-index multimode fibers having attenuation in the wavelength region around 0.85 µm of 3-5 dB/km and signal bandwidth of 500-1000 MHz.km;
- semiconductor lasers emitting at the wavelength of 0.85 µm with life at room temperature well established to reach 10.000-20.000 hours, and with extrapolations from high-temperature ageing tests indicating the feasibility of lifetimes in excess of 10^6 hours;
- silicon avalanche photodiodes providing internal photocurrent gain by a factor of 100 with excess noise relative to primary photocurrent shot noise less than a factor of 3-4;
- fiber coating and cabling techniques to make multifiber cables, capable of withstanding the forces exerted during pulling into ducts or laying in the ground;
- tools and techniques for easy and low-loss jointing of the optical fibers and for coupling the fibers to devices.

Fiber attenuation at the wavelength of 0.85 µm will probably be further reduced to a level of 2-3 dB/km. Laser output power launched into the fiber, now at a level of about 1 mW, will probably see an increase to a level up to about 10 mW.

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Systems and applications

The potential technical and economic advantages of glass-fiber optical transmission systems as compared to copper-based systems are rapidly coming to practical realization. Examples are found in the main fields of application.

a) Digital transmission between telephone exchanges. In many countries field trial installations, for digital transmission between telephone exchanges, are now in operation. Both industry and telecommunications administrations are putting up large efforts, and many more trial systems for this application will come into operation over the next couple of years. These systems carry from several hundred to several thousand digitally multiplexed telephone channels per fiber, and reach distances of 5-10 km before amplification and regeneration become necessary. The large capacity per fiber and, moreover, the possibility of putting a great number of fibers together in a relatively thin and low-weight cable combine to present a highly attractive way of providing increased traffic capacity. This is particularly urging in cities with crowded cable ducts and limited possibilities for construction of new ducts. The large repeater spacing obtainable with optical transmission furthermore reduces the expense for line equipment and in many cases makes underground repeaters unnecessary altogether. The coming years will probably see a strongly increasing effort towards industrial production and towards rapid introduction of optical systems in actual commercial service.

b) Wideband communication for individual subscribers. The often-mentioned possibilities of providing more and perhaps wideband services to individual subscribers depend in part on the availability of means for transmission. This holds in particular for visual communication services. Glass-fiber optical transmission has been mentioned as one means of making the necessary bandwidth available to the individual subscribers at relatively low cost.

Currently in a number of countries exploratory studies are being made, and even first experimental systems have already been installed. Major questions that remain to be resolved concern as much the precise nature of the new services as well as the optimum network and cable--system configuration by which those services are to be provided to the subscribers. Interfaces at the subscriber

station are of dominant importance in systems design. Both analog and digital transmission are in the picture for this application of optical-fiber transmission.

c) Data transmission in industrial plant. Optical-fiber transmission is rapidly finding its way in a great number of applications, a.o. in industrial control systems, where specific properties of optical fibers, especially electrical isolation and insensitivity to electromagnetic interference, offer important advantages. Electric power companies have been quick in noting the potential, and several glass-fiber systems for data transmission have already been put into operation.

At the same time, many system studies are being made concerning the use of optical-fiber transmission for interconnection of data processing equipment. Novel concepts appear to be feasible. An example of developments in this area is a high-data--rate looped optical bus system for interconnection of several independent data processing stations.

Circuit techniques

The optical transmitters and receivers in present optical communication systems are of relatively straightforward circuit design. In the transmitter, the semiconductor lightsource is directly driven from an electronic circuit; in the receiver, the semiconductor lightdetector is followed immediately by an electronic amplifier. All-optical circuitry is being thought of, but is not yet available for use in systems. Yet, although circuit design for present optical transmitters and receivers appears to be straightforward, special techniques will need to be further developed to make designs more compatible with existing electronic practice.
Examples are found in

- Feedback loops for stabilization or linearization of transmitter characteristics. Feedback schemes require that part of the optical power launched into the fiber be tapped off. Special devices are needed for this purpose. They introduce opto-mechanical complexity of micron precision;
- Stabilization and control of avalanche gain in avalanche photodiodes. Operating voltages of a few hundred volts add a high-voltage dimension to an otherwise low-voltage environment;
- Coupling of fibers to photodiodes and, especially, to laser diodes and light-emitting diodes. This requires micron-mechanical precision and needs to be realized in packaging designs compatible with available circuit techniques.

The coming years will probably see a development, first from isolated components gradually becoming compatible with printed-circuit board techniques, and next to circuits exhibiting an increasing degree of hybrid integration of opto-electronic and opto-mechanical components with the surrounding electronics.

New options for systems

The transmission window in fiber attenuation as a function of wavelength at around 0.85 µm and the availability of semiconductor light sources emitting in that wavelength region has been a fortunate coincidence which has in fact enabled the rapid progress towards operational systems. A transmission window exhibiting even lower fiber attenuation exists in the wavelength region of 1.1-1.3 µm. Due to lower intrinsic Rayleigh scattering, attenuation figures as low as 0.5-1 dB/km can be realized there. If suitable light sources and detectors for that wavelength region can be realized, transmission over distances up to several tens of kilometers will be possible without repeaters. Exploratory research has shown that suitable sources can indeed be made for this wavelength region. Both lasers and incoherent light-emitting diodes have already been realized. With further research suitable detectors probably can also be found. A further fortunate coincidence is that chromatic dispersion in the fibers almost disappears in this wavelength region. Thus, large repeater spacings can be obtained even with incoherent light-emitting diodes despite their relatively wide spectral width. The coming years will see further developments, including work on high-bitrate transmission via monomode fiber. Becoming noticeable now already is the desire for keeping open the option of later operation of systems at longer wavelength by ascertaining that presently produced fibers do indeed exhibit the low attenuation at the longer wavelengths.

Another option in optical communication systems which is getting increasing attention is that of multiple-wavelength operation. The signals from different transmitters, each operating at a different wavelength, are optically combined and sent along the same fiber. At the receiving end the different signals are separated spatially according to wavelength, e.g. by means of a prism, and fed to corresponding receivers. This systems option does require availability of light sources having a range of well-controlled wavelength settings. Multiple-wavelength transmission can have great merits for more complete utilization of fiber capacity and for doing away with high-speed electronic multiplexing and demultiplexing of signals. The coming years may be expected to see further exploration of the idea.

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TRENDS IN DYNAMIC RAMS

K. Hoffmann, K.U. Stein

Introduction

MOS-RAMs are best known for their high memory capacity and their cost advantage, as compared to other random-access memories. For the semiconductor producer RAMs are the leading products for technological advancements and for the user key elements used in all kinds of computers. Therefore, dynamic RAMs amount to 20% of total MOS sales, which are estimated to be 1800 Million US $ worldwide in 1978 /1/. The status and the future developments or those memories will be the topic of this presentation.

Status of dynamic RAMs

The highest bit capacity of all semiconductor RAMs has been achieved in the past ten years with dynamic MOS RAMs through the simultaneous advancement of circuit techniques and process development. This led to the most sophisticated RAM in volume production, the 16K-RAM /2,3/. It uses one-transistor-cells in double poly technology with an area as small as 450 μm^2 and dynamic sense amplifiers able to detect signals typical around 100 mV. The rapid development of dynamic RAMs has also caused a cost reduction by a factor of about 30 : 1 in the past decade /4,5/. Thus cost reduction, increase in volume production and technical improvements have been mutually enhanced. One goal of technical improvement was to develop more user friendly memories. The first 1K-RAM needed high voltage levels and had a current-sink-output. The 4K-RAM, which followed, was TTL-compatible at data and address inputs but required a 12V clock-pulse.
The next version of the 4K-RAM was address multiplexed and fully TTL-compatible. With the introduction of address multiplexing for 4K- and 16K-RAMs it was possible to place the dynamic RAMs into low-cost 16-pin packages which allowed further cost reductions due to the area-saving layout of p.c. boards. The omission of power-supply pins (3 pins at present) promises even 64K-RAMs /6/ and 256K-RAMs in 16 pin packages. Further progress was achieved by the continued performance improvements of the RAMs: the typical access-time has been reduced from 250ns for the 1K-RAM to 200ns for the 16K-RAM despite the 16-fold increase in memory capacity.

Trends of dynamic RAM developments

If the forecast of the memory-capacity evolution is done by extrapolating the past starting 1970 a quadrupling of the bit capacity approximately every 3 years (Fig. 1) /7/ can be predicted and a 1024KBIT memory could appear in 1985. To analyse the next steps of the development a review of the cell area decrease versus memory capacity as shown in Fig. 2 is useful. What can be seen is that the cell size has been reduced by a factor of about two at each new RAM generation. Steps in this reduction have been achieved by new cell structures and new technologies. Between these steps a gradual improvement of technology allowed a shrinking.

In the beginning of the RAM development the main emphasis was to decrease the cell size. This was obvious since the minimum cell area C_A was much larger than the minimum possible line pitch area P_A determined by the wordline driver and sence amplifier spacing (Fig. 2). This changed with the introduction of an additional poly-silicon layer in the cell of the 16K-RAM where the cell size C_A is almost as large as the line pitch area P_A. In the case of the announced 64K-RAM developed in VMOS-technology /6/ the cell area C_A is already smaller than the area P_A. Since the optimum silicon area utilization of a chip is achieved when $C_A = P_A$ it can be predicted that beyond this point the development will be determined primarily by scaling down existing structures unless a new concept is invented which reduces the cell size and the peripheral circuits simultaneously. The past efforts to achieve a better area utilization are shown in Table 1.

Considering the previous arguments it seems appropriate to analyse the future rate of scaling in more detail. Scaling is a concept that concerns coordinated changes in dimensions, voltages and doping concentrations /8/. A simplified summary of the scaling properties are shown in Table 2. Tremendous efforts are necessary to improve the technology from fine-line photolithograph to device properties and to deal with the complexity caused by the gigantic number of components in the design /9,10,11/. As for the near future until about 1985 the determining scaling rate factor will be the progress in photolithography. It is thus useful to consider the feature size (line width, spacing etc.) development of dynamic RAM's (Fig. 3) in some detail. The minimum feature size (D_{MIN}) for each new RAM generation has gradually shrunk in the past /12/. This tendency will be continue in the future utilizing the new photolithography techniques presently under development /13/. Two steps seem to be feasible for the feature size range from 3µm to 1.5µm the projection printing /14/, and range below 2µm the electron beam, deep UV or X-ray writing /11/. If one extrapolates from the past that for yield purposes the chip size will not increase remarkably for future dynamic RAM's, a feature size reduction as shown in Fig. 3 together with the relevant photolothograph techniques is required. This development correlates very well with Moore's feature size projection in 1975 /15/.

Conclusion

The previous analysis has shown, that the rapid development of dynamic RAM's, which has caused a quadrupling of the memory capacity approximately every 3 years may continue beyond the 64K-RAM. The development which governs this progress will primarily be determined by the scaling rate of existing technologies rather than by new technologies or circuit techniques. This means that the dynamic RAM remains a key component and will determine furthermore the technological progress in the future.

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References

/1/ DATAQUEST, 24 Apr. 1978

/2/ Ahlquist, C.N. et al:
A 16384-bit Dynamic RAM.
IEEE J. Solid-State Circuits,
Vol. SC-11 (1976), No. 5, pp 57Q-574.

/3/ Mitterer, R.W., Rehn, B.F.:
A 16K-MOS-RAM- with double-polysilicon technology.
Tagungsband ESSCIRC, Toulouse (1976), S. 40-41.

/4/ Garbrecht, K., Stein, K.U.:
Perspectives and Limitations of Large-Scale Integration.
Siemens Forsch.- u. Entwickl.Berichte,
Bd. 5 (1976), Nr. 6.

/5/ Mitterer, R.W.:
Grossintegrierte Halbleiterspeicher.
In Proebster (Ed): Digital memory and storage,
Vieweg, Braunschweig, 1978.

/6/ Hoffmann, K., Losehand, R., Zapf, K.:
VMOS Dynamic RAM.
1978 IEEE Solid-State Circuit Conf. Vol. XXI,
IEEE Cat No. 78 CH 1298-9.

/7/ Coe, J.E., Oldham, W.G.:
Enter the 16, 384-bit RAM.
Electronics, 19 Febr. 1976.

/8/ Dennard, R.H. et al:
Design of Ion Implanted MOSFET's with Very Small Physical Dimensions.
IEEE, J. Solid-State Circuits, SC-9,
pp 256-268 (Oct. 1974).

/9/ Folberth, O.G., Bleher, J.H.:
Limits of Digital Semiconductors Technology,
Nachrichtentech. Zeit., 30 pp 307-314 (1977),
in German.

/10/ Swanson, R.M., Meindl, I.D.:
Fundamental Performance Limits of MOS Integrated Circuits. 1975 IEEE Intern. Solid-State Circuits Conference, Digest of Tech. Papers,
pp 110-111.

/11/ Rideout, V.L.:
Physical and Electrical Limitations to Improvement of Silicon Integrated Circuits.
IEEE Workshop on Large Scale Intergrations.
Stanford University. 22 Apr. 1978.

/12/ Stein, K.U.:
Technologischer Stand und zukünftige Entwicklung in der Mikroelektronik. Elektrotechnik und Maschinenbau, Jahrgang 93, Heft 6.

/13/ Special issue on pattern generation and microlithography,
IEEE Transactions on Electron Devices,
Vol. ED-22, No. 7, July 1975.

/14/ Rosen, B.M.:
Direct Step on Wafer takes off.
Morgan Stanley Electronics Letter, 27 Apr. 1978.

/15/ Moore, G.E.:
Process in Digital Integrated Electronics,
IEDM Tech. Digest (1975), pp 11-13.

/16/ Stein, K.U., Sihling, A., Doering, E.:
Storage array and sense/refresh circuir for single transistor memory cells. IEEE J. of Solid-State Circuits, Vol. SC-7, No. 5,
Oct. 1972

/17/ Heller, L. et al:
High sensitivly charge-transfer sense amplifier.
Proceedings of the ISSCC 75, Febr.1975,
Philadelphia.

/18/ Heller, L., Spampinato, D., Yao, Y.:
High sensitivity charge-transfer sense amplifier.
IEEE J. of Solid-State Circuits, Vol. SC-11,
No. 5, Oct. 1976, pp 596-601.

/19/ Hoffmann, K.:
The behavior of the continuously charge-coupled random-access memory (C^3RAM).
IEEE J. of Solid-State Circuits, Vol.SC-11,
No. 5, Oct. 1976, pp 591-596.

/20/ Schroeder, P.R., Proebsting, R.J.:
A 16K x 1 Bit Dynamic RAM.
1977 IEEE Solid-State Circuits Conference,
Vol. XX IEEE CAT No. 77CH 1172-6.

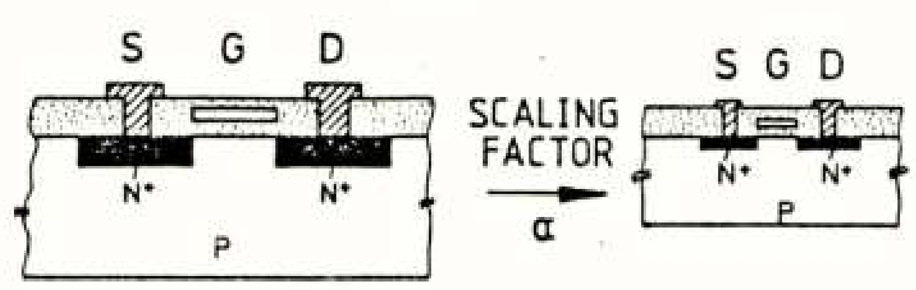
/21/ Tasch, Al.F. et al:
Charge capacity Analysis of Charge-Coupled RAM Cells.
IEEE J. Solid-State Circuits, Vol. SC-11
(1976), No. 5, pp 575-585.

/22/ Lee, H.S., Pricer, W.D.:
Merged Charge Memory (MCM) - a new Random Access Cell.
IEDM Techn. Digest (1976), pp 15-17.

/23/ Horninger, K., Meusburger, G., Keller, H.:
Stacked-Electrode Dynamic Memory Cell in Double Polysilicon Technology.
ESSCIRC 1977, Digest of Techn.Papers, Sept.
20-22, 1977.

Areas of improvements	Reference
Signal Sensing	
Sense / refresh circuit	[16]
Charge - transfer sense amplifier	[17,18]
C^3 RAM	[19]
Dynamic sense amplifier	[20]
Storage Cell	
CC - RAM Cell	[21]
MCM - Random Access Cell	[22]
Stacked - Electrode Dynamic Cell	[23]

Table 1



SUBSTRATE DOPING	α
LATERAL AND VERTICAL DIMENSION	$1/\alpha$
SUPPLY VOLTAGES AND CURRENTS	$1/\alpha$

COMPONENT DENSITY	α^2
POWER DISSIPATION	$1/\alpha^2$
DELAY TIME	$1/\alpha$
POWER - DELAY PRODUCT	$1/\alpha^3$

Table 2

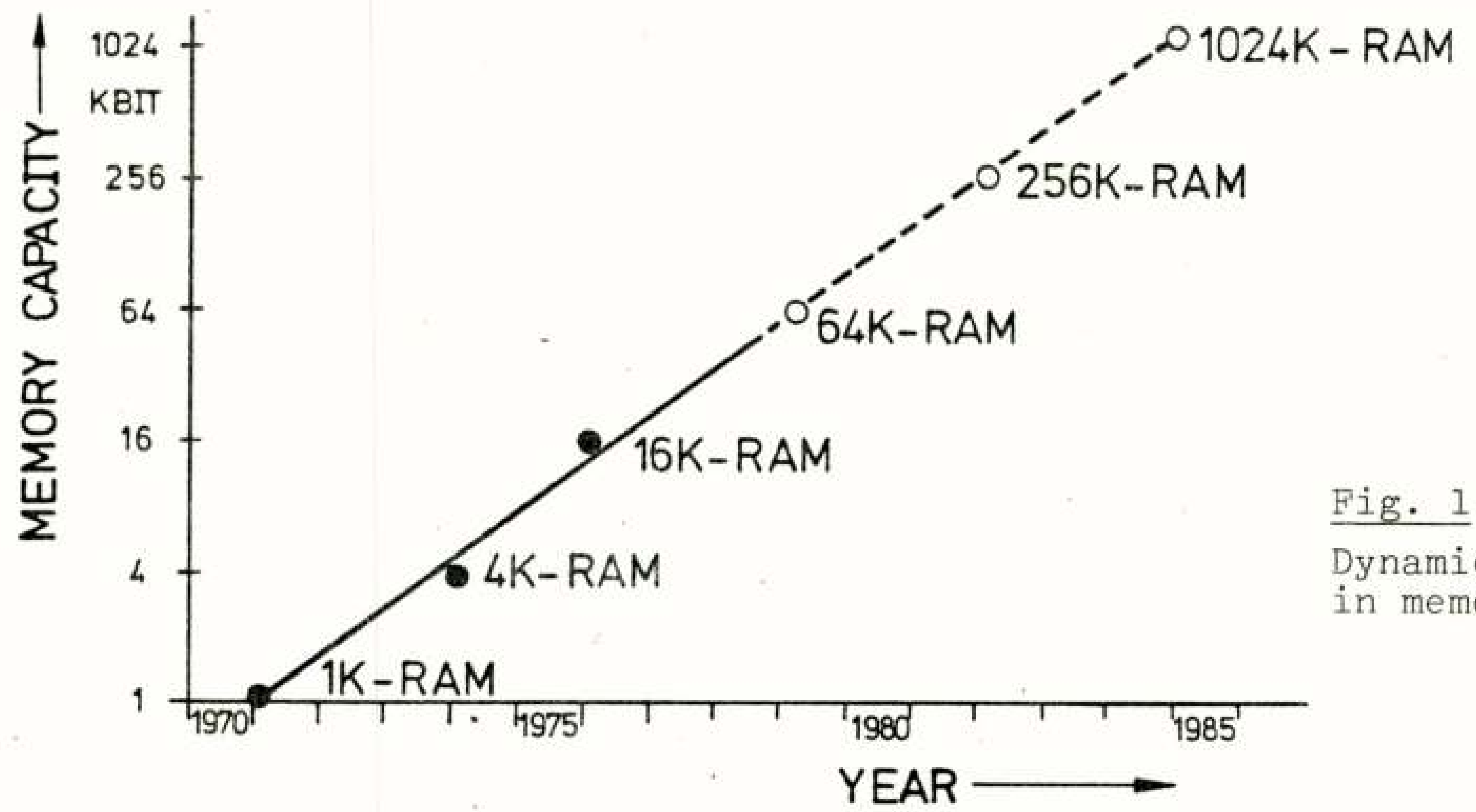


Fig. 1

Dynamic RAMs increase in memory capacity

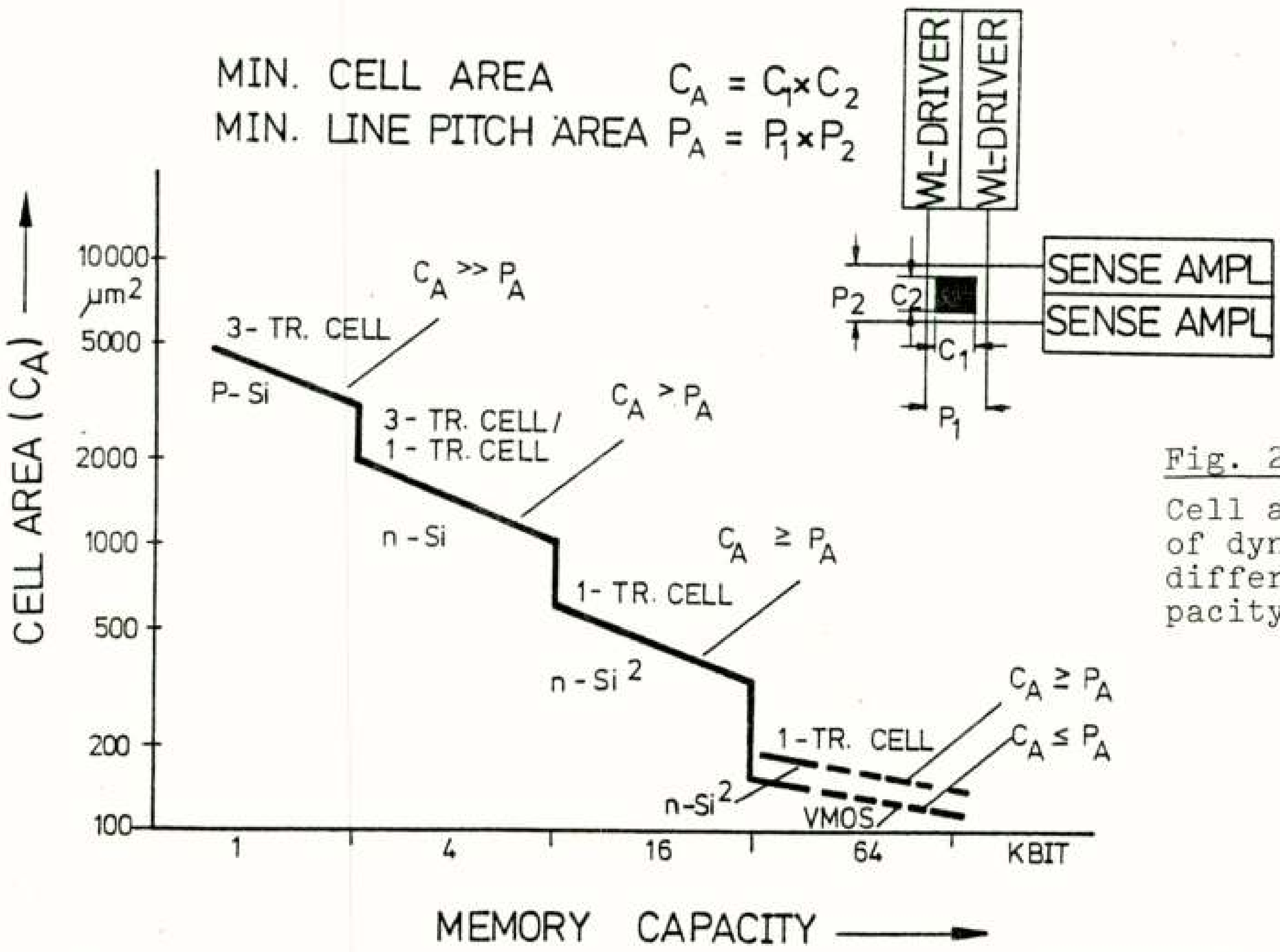


Fig. 2

Cell area development of dynamic RAMs with different memory capacity

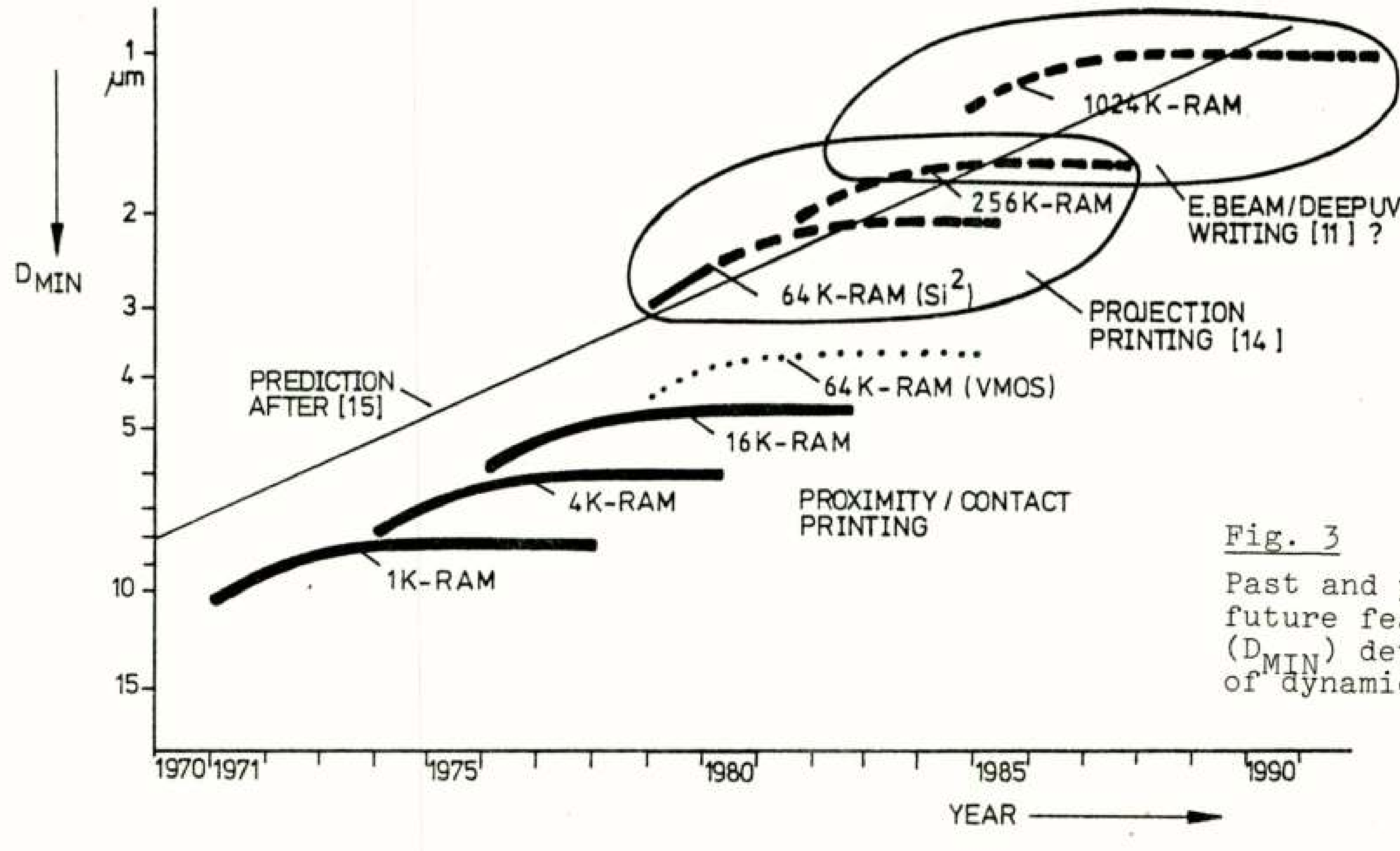


Fig. 3

Past and possible future feature size (D_{MIN}) development of dynamic RAMs

MEMORIES WITH JOSEPHSON JUNCTIONS

P. Wolf

Abstract

The talk is based on an overview which was published recently (1). For this reason, only an abstract is given here, which includes later results not contained in the aforementioned overview.

The presently-known Josephson memory cells store information as persistent currents in superconducting loops, or what is equivalent as a magnetic flux in the area of the ring. This method of storage is nonvolatile and has no power consumption in the storing state. In a superconducting ring system, the magnetic flux is quantized, and cells have been built which operate either with only one flux quantum, or with many of them.

For the latter cells with many flux quanta (ring cells), quite a number of designs exist. They have one or two Josephson junctions in the ring, which allow writing. An external junction which is controlled by the ring current serves for non-destructive reading of the information. The smallest cell realized had an area of 900 μm² with a 2 μm minimum line width. Switching speed was ≲ 80 ps.

Cells which store information as a single-flux quantum (single flux-quantum cells = SFQ cells) in the ring, usually contain two Josephson junctions used for reading and writing. Read-out in most of these cells is destructive, but methods of reading non-destructively have also been proposed. The smallest device made had an area of ≈ 150 μm² with a minimum line width of 2 μm. The read signal had a rise time ≲ 100 ps.

Recently, experimental memory models have been published with both types of cells. In these models, the drive and decode circuits use current steering in superconducting loops, with Josephson junctions as switches.

The experimental model (2) with ring-type cells contains an 8 × 8 array and is fully decoded. Worst-case access time is about 4 nsec.

The largest model (3) made so far was built with an array of 2000 single flux-quantum cells and part of the required drivers and decoders. It was realized to test the electrical feasibility of a 16 kBit memory chip. The results obtained indicate that such a chip is electrically feasible and would have an access time of ≈ 15 nsec and a power consumption ≲ 40 μW.

In summary, work on Josephson memory devices shows that not only cells, but, also full memory chips with drivers and decoders are feasible. These memories combine high speed with very low power-consumption.

References

(1). P. Wolf, in "Digital Memory and Storage", W.E. Proebster (Ed.), Vieweg, Braunschweig, 1978.

(2). W. Henkels and H.H. Zappe, IEEE J. Solid-State Circuits, (to be published).

(3). R.F. Broom *et al.*, IEEE 1978 International Solid-State Circuits Conference, San Francisco, Digest of Technical Papers, p. 60.

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COMPUTER AIDED DESIGN : TRYING TO BRIDGE THE GAP.

Hugo De Man,

Introduction

As a result of the evolution of I.C. technology over the past two decades, component complexity has increased from one single to over 20.000 transistor functions per chip with usually less than 100 testable outputs.
Low cost per logic operation or unit storage has resulted in predominantly digital components with occasionally small peripheral A/D and D/A interfaces potentially on the same chip. Low cost of such single chip systems is only possible by reducing design cost/function and avoiding cost penalties for designs errors. Therefore Computer Aided Design (CAD), more than ever before, has become an absolute necessity in a VLSI design environment.

In this paper the different CAD disciplines involved in IC design will be considered and their evolution will be compared to the evolution of todays IC design complexity.
Development of LSI has created distributed computing power which in term has influenced CAD system. On the other hand CAD, especially testing design, may have an influence on the design process itself and this will probably be the only way to bridge the gap between technology and design software. These points will also be discussed.
Fig. 1. illustrates a possible "integrated" VLSI design system. It consists of eleven CAD disciplines of which numbers (1)* through (7) coincide with the top-down bottom-up design process. The large number of feedback loops account for the well known "iterative design
They are a clear indication of the need for items (8) and (9) i.e. a common data base and a common hierarchical description (I/O) language in order to avoid error prone recoding of different activities in the design process.
The activities of technology (10) and device modeling (11), although not directly involved in the chip design, have been and certainly will be essential to create an understanding of new VLSI processes and to generate in (8) compact submicron device models suitable for use in (4) and (5). To our knowledge no such system exists yet but all items (1) through (11) are in full evolution and will be examined. An overview of the problems related to (10) and (11) can be found in [48].

State of the art of CAD disciplines and their evolution.

a) Circuit simulation.

Up to 1972 the most complex design problems were in the analog field. Digital MSI circuits (TTL, CMOS) were conceptually simple and usually contained less than 100 devices. Therefore electrical (sub) circuit simulation (4) (ECAD) was the most widely used CAD tool in IC design. Since 1968 numerous such ECAD programs have become commercially available [1-5] These programs allow for very accurate DC, AC, time domain, noise and sensitivity analysis based on the well known nonlinear circuit models for bipolar and MOS transistors [6-12] valid down to todays 4 μm line widths and directly linked to technology and geometry [11 13 14]. A careful comparison of such programs [15] indicates that since 1973 no significant advances have been made. Most ECAD programs are limited to a maximum of 400 nodes and a few hundred transistors requiring ca. 150 Kbyte of memory. Furthermore, as shown in Fig. 2., time domain simulation cost increases quadratically with circuit complexity. This is an inescapable result of the general use of sparse matrix techniques, Newton-Raphson iteration and implicit integration with time step control. Fig.2. illustrates clearly that the use of ECAD as such is totally ineffective for full the simulation of (V)LSI circuits. It is however, as shown in Fig. 1., an ideal tool during early stages of LSI design when the chip is parthioned into subcircuits containing fifty transistors or less. Since, especially for MOS, a clear link of device models to geometry [9][14] exists, Fig.1. suggests a direct coupling of ECAD to "manual" layout i.e. graphic display with tablet. Often graphic displays are operated in conjunction with a minicomputer which in itself can be used as an intelligent terminal of a maxicomputer. Therefore recent developments in ECAD tend towards efficient minicomputer [16 ... 17] and even programmable disktop calculator [18] programs capable of analyzing 50 transistor circuits within 32 Kwords of 16 bits. Larger complexity is automatically handled by a maxicomputer. Subcircuit simulation of this kind is highly interactive and allows for the accurate verification of functional block specification (time delay, stability, temperature behavior, tolerances) and the design of data base stored macromodels for logic, timing and test verification to be discussed below.

b) Digital systems simulation (9)(5).

With the advent of I^2L and MOSLSI, chip complexity rapidly exceeded classical ECAD simulation limitations. Integrated circuits now are at systems level and therefore, about five years ago, IC designers started to look into the tools developed by digital systems (computer) designers i.e. systems- and logic simulation as well as testpattern generation and verification.
In contrast to electrical simulation logic simulation does not operate at voltage and current level but on states of the signal paths or nodes. Models are not at device level but at gate, register, memory level. They are logical operators on the algebra of signal states and have more or less sophisticated delay description [19][20][21 Chpt. 4]. Fig. 3. illustrates how for example a NAND gate operates on the 1,x,o signal set. Logic simulators therefore operate totally different from ECAD. They are table and event driven [19] . An event is defined as a change of state of a signal path. As shown in Fig. 4. an event is propagated to its fan-out, where usually only a restricted number of new events have to be scheduled in future event lists. Following the scheme shown in Fig. 4. we see that at a given time only those gates active at that time are evaluated. In most large digital systems this number is less than 1% of all gates. This technique is called selective trace [37] or latency exploitation.

* Numbers in parenthesis refer to activities in Fig.1.

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From the above it follows that logic simulation is 3 to 4 orders of magnitude more efficient in execution time than existing electrical simulation and 2 to 3 orders more efficient in terms of storage requirements for the same circuit function. Fig. 5 [20] illustrates the trade-off between circuit complexity and simulation tool indicating that logic simulation can handle todays LSI complexity but perhaps not tomorrows full VLSI chip.
Logic simulation has been used succesfully for design and timing verification of PCB designs using well standardized MSI packages.
Dependent on the layout system used, however, seldom such standardization is present in LSI design, especially when high volume production is envisioned. This explains why layout coupled ECAD at low complexity levels is needed to generate macromodels with associated local delay for logic simulators as shown in Fig.1.
Furthermore in memory and dynamic MOS logic design a large number of design problems result from such "electrical" and layout dependent effects as clock-feedthrough, charge sharing, transfer gates, etc... which cannot be taken into account by logic simulators, while on the other hand circuit complexity is too high for ECAD.

To fill this gap recently a number of CAD tools [23] [24] [25] [26] have appeared, capable of coping with those electrical effects at complexity levels up to a few thousand gates. This discipline is now called "timing simulation".
The efficiency of timing simulation is based on the following facts :
- device nonlinearities are handled as stored tables [24] [25] or as network elements controlled by Boolean variables [26] rather than as arithmetic functions. - latency and selective trace are exploited as in a logic simulator. This can be done by equation decoupling for small timesteps [24] [26] or by tearing methods for modular networks [27].
In this way matrix inversion as well as nonlinear iteration is avoided with little loss in accuracy but ca. 2 orders of magnitude increase in efficiency.
- The use of electrical macromodels to model at gate or flip-flop level [29] [30] [31] [32].
As a result timing simulators are ca. two orders of magnitude faster than ECAD [24] [28] [32] and allow typically for a simulation speed of 0,5 ... 5 ms/gate/timepoint for circuit up to 2000 gates (see also Fig. 5).
Recent developments [28] [32] indicate that the introduction of logic simulator data structures into ECAD and timing simulators will leed in the coming years to a compatible mixed electrical-timing-logic simulator package which is capable of simulating LSI circuits up to 3000 gates described from functional to transistor level, dependent on the accuracy requested by the designer. It is clear from Fig. 1. how such a system with a common structural design language [33] fits into an LSI design system. Fig. 5. indicates that today only logic simulation at the lowest signal level (0,1) can cope with the 10.000 gate complexity as soon expected in VLSI. Higher complexity can only be simulated at byte and word level. The latter is called systems simulation and performs simulation of the concept of the system, starting from the functional structure of it. An example of such simulator is the CASSANDRA program [34]. An overview of system description languages can be found in [35]. Due to lack of standardization and lack of education of designers not much use is made yet of systems simulation software although it may become necessary in a few years [36].

c) CAD for testing (7).

Perhaps the biggest problem facing (V)LSI is the problem of testability. Testing consists of applying a sequence of inputs to a circuit (test pattern), observing the response at a (limited) number of testable output pins and comparing it with a precompared "expected" sequence. Cheap testing is a prerequisite for low cost LSI circuits.
The test problem consists of two parts : testpattern generation and test verification. The latter consists in computing how many physical faults (usually stack-at faults) are covered by a given test input. This problem can be solved using logic simulators either in the parallel mode [20] [38] or the deductive mode [39] [40]. In the first method a subset of the total number of "faulty" circuits proportional to the word length of the host computer, are simulated together with the good one. A full fault simulation thus consists of a large number of separate simulations. In the second method the full fault list is "propagated" through the network in one single simulation.
The latter method seems most appropriate for complex sequential circuits although it requires a large memory computer to execute. Notice that even when operating at (1,0) level (fig.5) we are limited to ca.10K gates.
Although in the past test patterns have been generated manually, this method cannot go on for complexities over 500...1000 gates. Therefore automatic test pattern generation (ATPG) algorithms have been proposed. Of these methods Roth's D-algorithm [41] based on path sensitization is most widely used. Other programs use full output-input path sensitization to maximize the number of faults detected per test pattern [21]. This technique is implemented in the D-LASAR [42] program which generates test patterns exclusively for NAND gate network up to ca. 1...5K gate level (dependent on the nr. of sequential states). It has been shown however [43] that the known ATPG methods are at best polynomially complete such that there is not much hope that ATPG (at gate level) will be able to cope with VLSI complexity.
Therefore it becomes clear that in the area of testing, instead of adjusting CAD tools to the design, we will have to make the design accessible for CAD tools [22] [44].
It is indeed known that the structure of logic can have a strong influence on the complexity of testing [45] [46] while on the other hand, especially sequential circuits, can be made testable by making them operate, for test purpose only, as shift registers and combinational circuits [47]. An overview of such techniques can be found in [22]. It can therefore be concluded that the test problem in itself will probably have a profound influence on the architecture of future VLSI circuits since if testing is not taken as a design consideration, VLSI may soon become ILSI i.e. Impossible LSI.

d) CAD for Layout (CAL) (2)(3)(6).

Layout of integrated circuits ranges from fully "manual" layout, using a digitizer or graphic display to fully "automated" layout. This leads to a trade-off between chip-size and design time as illustrated in Fig. 6.
Most automated systems use a library of predesigned cells (operation (2),(3),(4) fig.1) and do an automatic placement and routing of the cells [49] [50] using an orthogonal net of two interconnection levels (6).
Once the full layout is obtained interconnection parasitics can be calculated and a timing and/or logic simulation can be performed for design verification. Sofar this technique is only being used for

quick turn-around custom LSI [51] due to the larger chip-size as shown in fig. 6.
A number of new techniques allowing for the introduction of large functional blocks (ROM, RAM, PLA etc...) [52], the use of cells with top and bottom interconnections [51] and higher level of interaction however is quickly reducing the difference between manual and hand layout. Such techniques reduce the vast problem of design rule checking [52] and logic diagram generation [53] to smaller subcircuits which are manually laid out at subcircuit level using symbolic layout techniques [54]. Symbolic layout can be automatically coupled to minicomputer ECAD by device recognition [53] [55].
This technique is in full agreement with the necessity to design future VLSI circuits with large modular blocks which is also a necessity for testing as discussed above.

References.

[1] L.W. Nagel,"SPICE 2: A Computer Program to Simulate Semiconductor Circuits",ERL Memo No.ERL-M 520,Univ. of Calif., Berkeley.

[2] -,"ASTAP General Information Manual",(6H20-1271-0),IBM Corp.,Mechanicsburg,Pennsylvania,USA.

[3] M. Heydemann, "ASTEC 3, A user oriented circuit analysis program",Abstracts of ESSCIRC 76,LAAS CNRS 7, 1400 Toulouse, France.

[4] -,"Users Manual for TRSIT",available from LISCO, Kard.Mercierlaan 94,Heverlee 3030, Belgium.

[5] -,"IMAG III Manual",Institut de Mathematique Appliquée de Grenoble, Grenoble, France.

[6] H.K.Gummel, H.C.Poon, Bell Syst. Tech. Journal, Vol.49,pp.115-120, Jan. 1970.

[7] J.Meyer, RCA Review, Vol.32,pp.42-63.

[8] Y.A.El Mansy,A.R.Boothroyd, IEEE Tr. on El. Dev., Vol.ED-24,pp.241-253, 1977.

[9] D.R.Alexander et al., "SPICE 2 MOS Modeling Handbook", BDM Corporation, 2600 Yale Blvd, Albuquerque 87 106, U.S.A.

[10] J.G.Ruch, Comptes rendus journees d'électronique 1977, Ecole Polytechnique de Lausanne, pp.89-118, Oct. 1977.

[11] H.Martinot, P.Rossel, see ref. 10 ,pp.153-284.

[12] I.Getreu,"Modeling the bipolar transistor",1976 Tektronix Inc. Beaverton,Oregon 97077, U.S.A.

[13] H.De Man, R.Mertens, ISSCC Digest of technical papers, febr.1973,pp.104-105.

[14] J.Compeers et al.,IEEE Trans.on El. Dev.,Vol. ED-24,pp.739-764, June 1977.

[15] -,"A Survey of computer-aided design & analysis programs", Electrical & Electronics Systems Dept., Univ.of South Florida, Tampa 33620, USA (Rpt.nr. AFAPL-TR-76-33).

[16] -,"Users manual of GENSIMI program",LISCO, Kard. Mercierlaan 94, 3030 Heverlee, Belgium.

[17] T.K.Young, R.W.Dutton, IEEE Journal of Solid State Circuits, Vol.SC-11, no. 3, pp. 730-732,Oct.76.

[18] A.R.Newton,A.L.Taylor, Conf.Record, 10th Asilomar Conf. on Cir.,Syst. and Comp.,pp.280-283,1976.

[19] S.A.Szygenda, E.W.Thomson, Computer,pp.23-36, March 1975.

[20] S.A.Szygenda, E.W.Thomson, Computer,pp.38-49, March 1975.

[21] M.A.Breuer, A.D.Friedman,"Diagnosis & Reliable Design of Digital Systems",Pitman Publ.Ltd., London,1977.

[22] M.T.M.Segers,"Design for testability",Proc. summercourse on CADLIS 1978,Univ.Leuven,Kard.Mercierlaan 94,3030 Heverlee, Belgium.

[23] N.B.Rabbat et al.,IEEE Tr. on El. Dev.,Vol.ED-22, No.8, pp.523-531, Aug. 1975.

[24] B.R.Chawla et al., IEEE Tr.on Circuits and Systems,Vol.CAS-22,pp.901-910,Dec. 1975.

[25] S.P.Fan et al.,Proc. IEEE Int'l Symp.on Circuits and Systems, pp.700-703, 1977.

[26] G.Arnout, H.De Man, Journal of Solid State Electronics,Vol.SC-13,No.3, June 1978.

[27] N.B.Rabbat,H.Y.Hsiech, IEEE Trans. on Circuits & Systems,Vol.CAS-23,No.12,pp.745-752,Dec. 1976.

[28] M.Y.Hseuh et al.,see ref. 10 ,pp.403-413.

[29] J.R.Greenbaum, Electronics, pp.121-125,Dec.1973.

[30] M.Glesner, see ref. 10 ,pp. 431-441.

[31] M.Y.Hseuh, D.O.Pederson,Proc. 1977 IEEE Int'l. Symp.on Circuits & Systems,pp.696-699,1977.

[32] H.De Man, G.Arnout, Proc.1978,IEEE Int'l.Symp. on Circuits and Systems.

[33] W.M.Van Cleemput, Proc.14th Design Automation Conf.,New Orleans,June 1977, pp.378-385.

[34] Bogo,Guyot et al.,Proc. of IFIP Congress,1971, Vol.TA-6,p.26, 1971.

[35] S.Y.Su, Computer, pp.45-51, Dec. 1974.

[36] S.Y.Su, Proc. 11th Design Autom.Workshop, Denver, Colorado,pp. 186-193, June 1974.

[37] E.G. Ulrich,Comm. of ACM,Vol.13,No.12,pp.102-110, Febr. 1969.

[38] H.Rombeek, P.Wilcox, Proc.13th Design Autom.Conf. San Francisco,pp.68-73, June 1976.

[39] D.B.Armstrong, IEEE Tr.on Comp., Vol. SC-21, pp.464-471, May 1972.

[40] H.Y.Chang,S.G.Chappel, Computer,pp.52-59,March 1975.

[41] J.P.Roth, IBM J. of Res. & Developm., pp.278-291, July 1966.

[42] J.J.Thomas, Computer Design,pp.63-67,Aug.1971.

[43] O.H.Ibarra, S.K.Sahui, IEEE Tr.on Comp., Vol.SC-24,pp.242-249, March 1975.

[44] M.J.Williams,J.B.Augell, IEEE Trans. Computers, Vol.SC-22,pp.46-60, Jan. 1973.

[45] J.P.Huges, IEEE Tr.Computers,Vol.SC-23, pp.56-62, Jan. 1974.

[46] K.K.Saluja, S.M.Reddy, IEEE Trans. Computers, Vol.SC-23,pp.552-554, May 1974.

[47] Several authors, Proc.of 14th Design Autom. Conf., pp.460-492, June 1977.

[48] -, Proc. of NATO Course on process and device modeling, Université Catholique de Louvain, Belgium, July 19-29, 1977.

[49] G.Persky et al., Proc. of 13th Design Autom. Conf., San Francisco, pp.399-416,June 1976.

[50] H.Beke, W.Sansen, IEEE Journal of Sol.Stat.Circ.

[51] A.Feller, Proc. 13th Design Autom. Conference, San Francisco, pp.79-85, June 1977.

[52] T.Kozawa et al., Proc. 11th Design Autom. Workshop, Denver, pp. 26-46, June 1974.

[53] B.W. Lindsay, B.T.Preas, Proc. 13th Design Autom. Conference, San Francisco, pp.307-308, June 1977.

[54] B.T.Preas et al., see ref. 52 ,pp. 309-317.

[55] D.Gibson, S. Nance, see ref. 52 ,pp.434-440.

[56] I.Dobes, R. Byrd, see ref. 52 ,pp. 327-335.

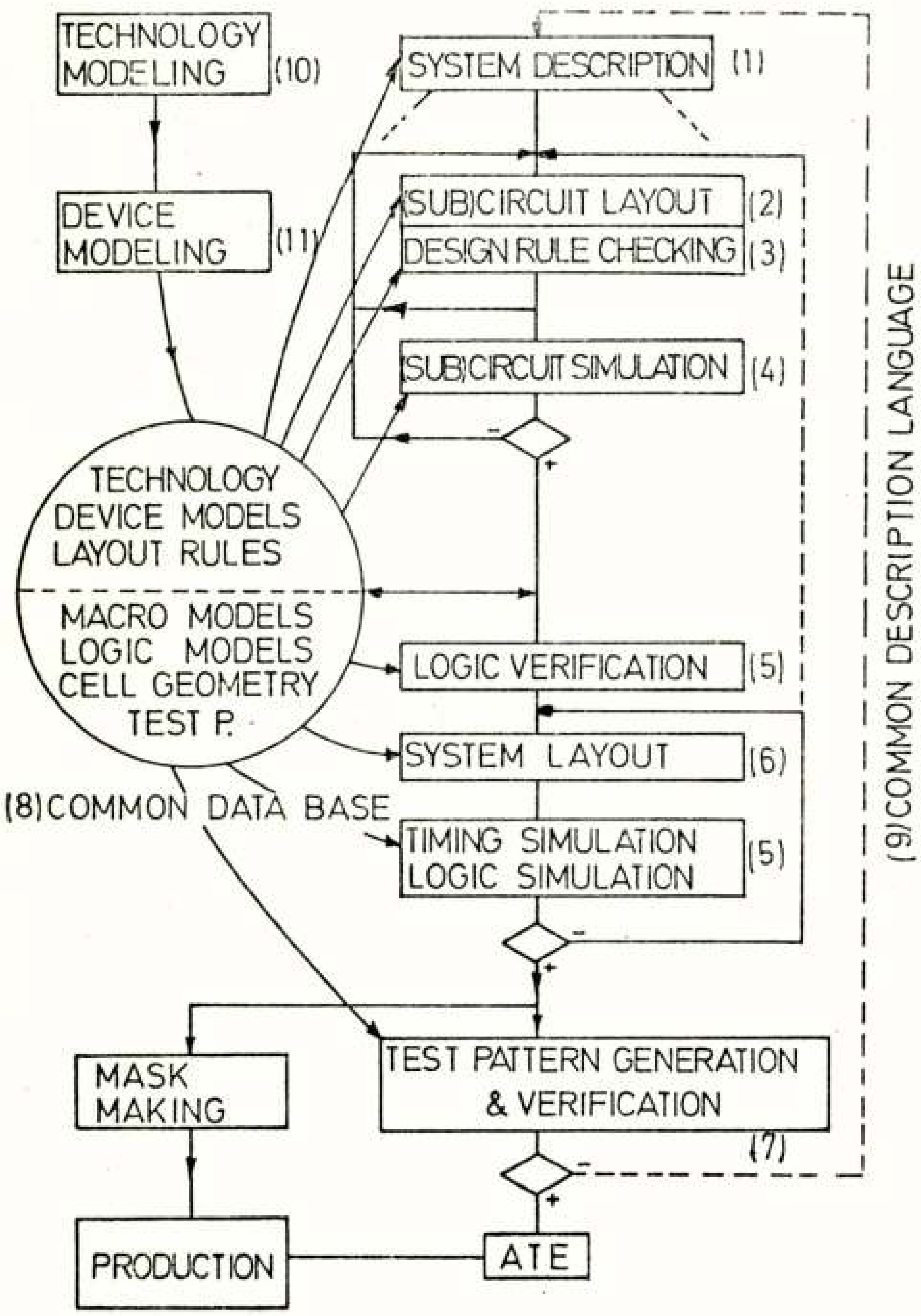


Fig.1. "Ideal" integrated LSI design system.

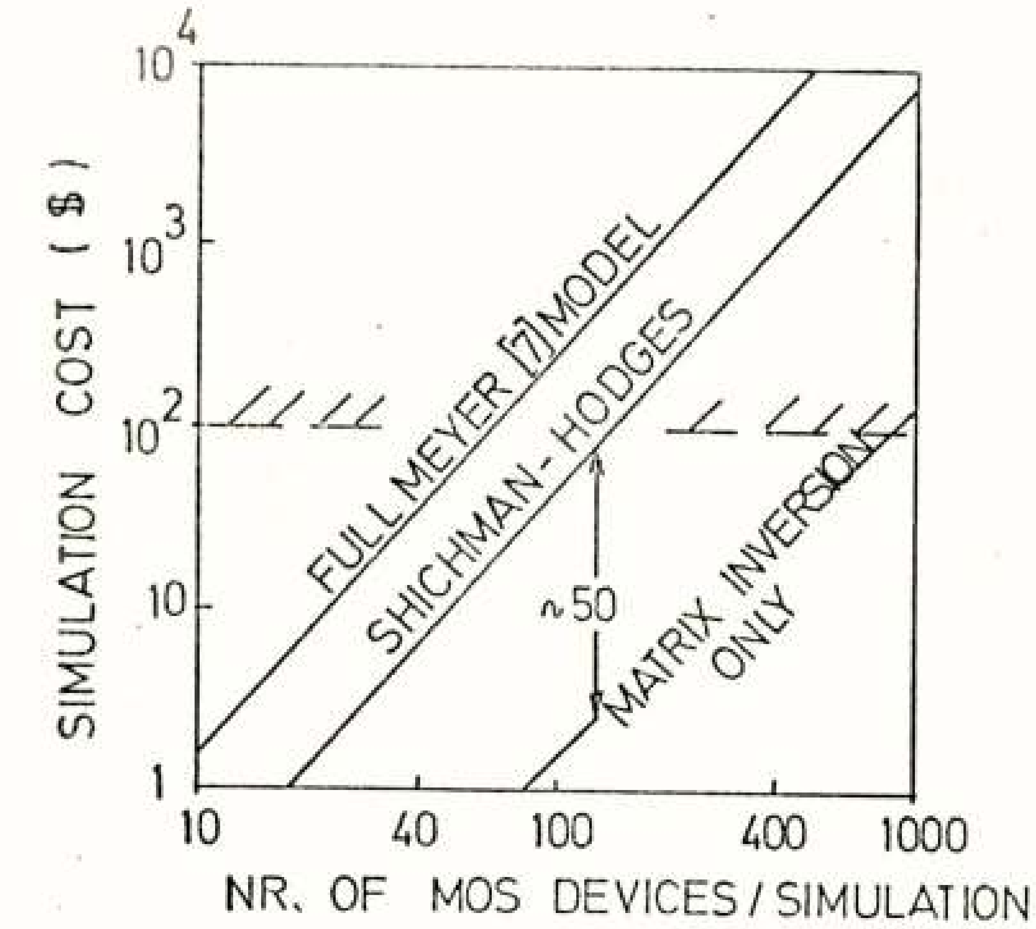


Fig.2. Simulation cost vs. circuit complexity for two MOS models. Hypothesis : IBM 370/158, TRSIT program, 1000 time points. Automatic time step control. Non-linearities cause large loss in efficiency.

A \ B	1	O	X
1	O	1	X
O	1	1	1
X	X	1	X

C for t = t + Δ

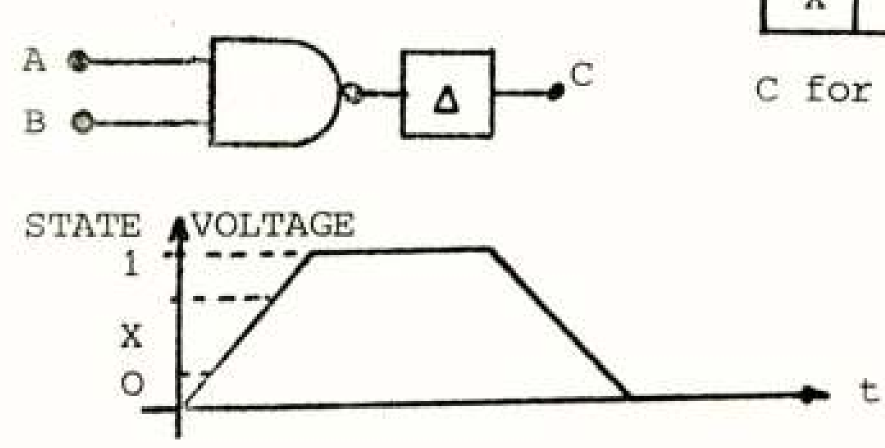


Fig. 3. Modeling of a NAND gate for logic simulation. Model is algebraic operator.

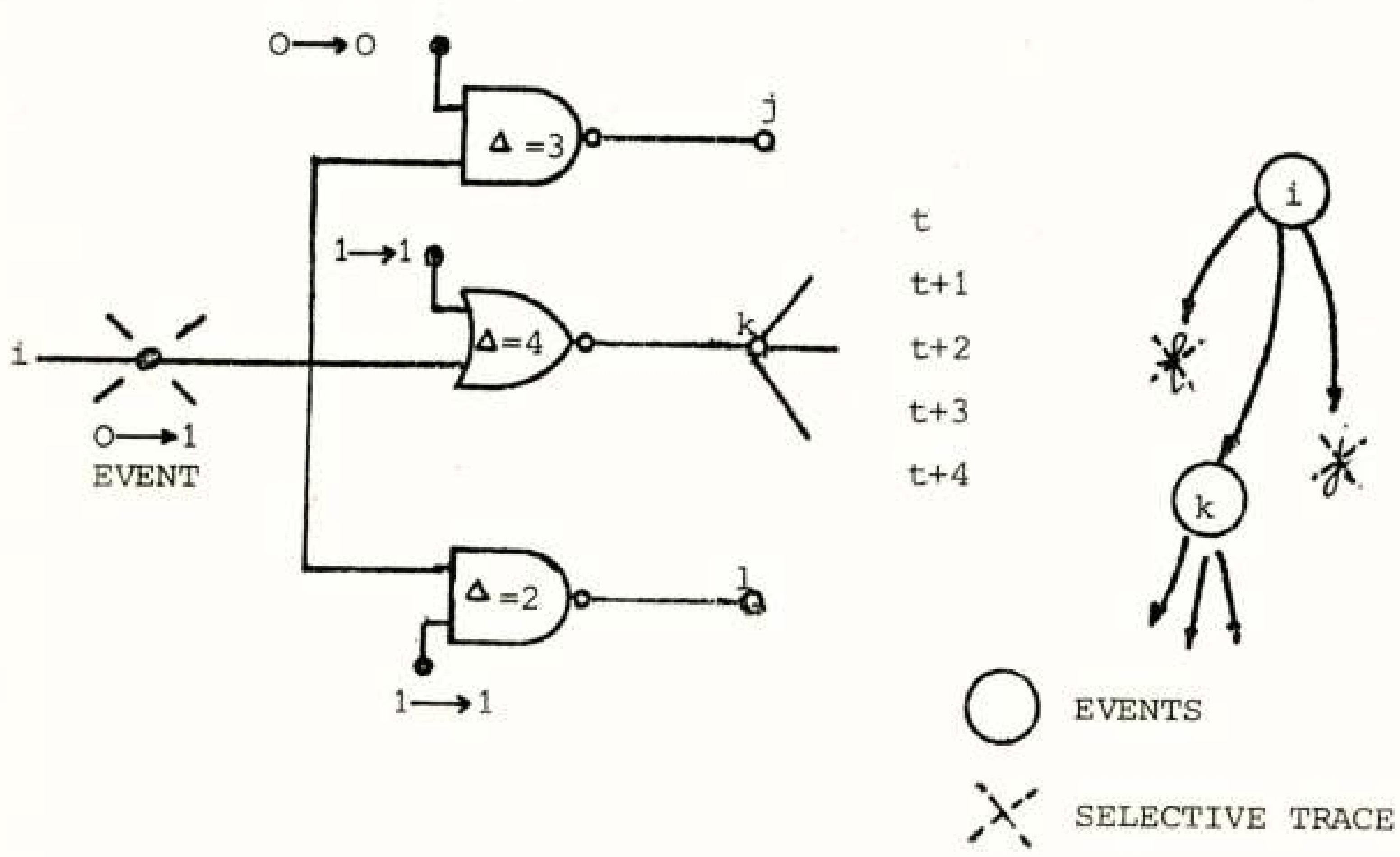


Fig.4. Illustration of event driven simulation with selective trace. Only active part is simulated.

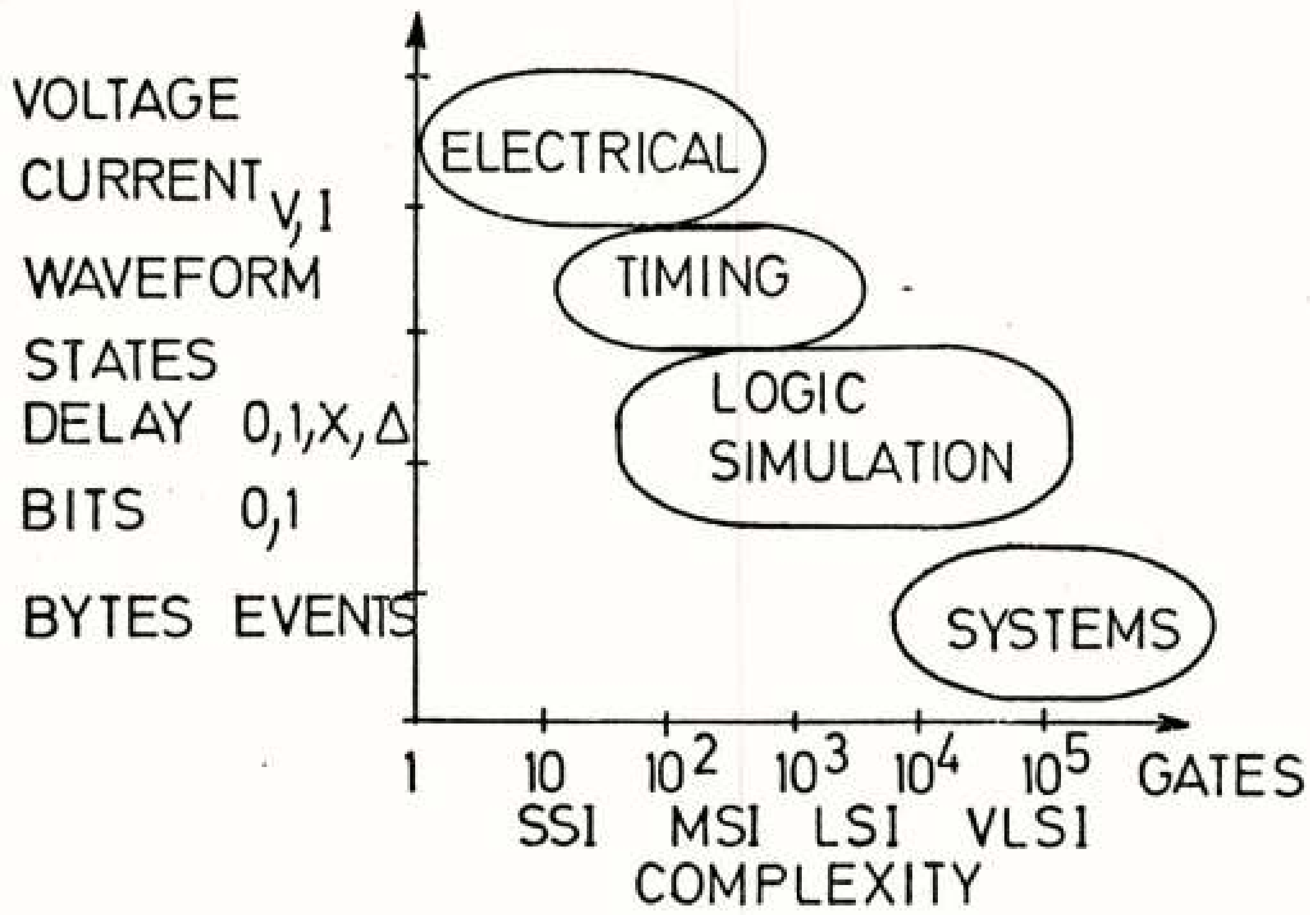


Fig. 5. Level of signal representation versus component complexity for comparable simulation costs.

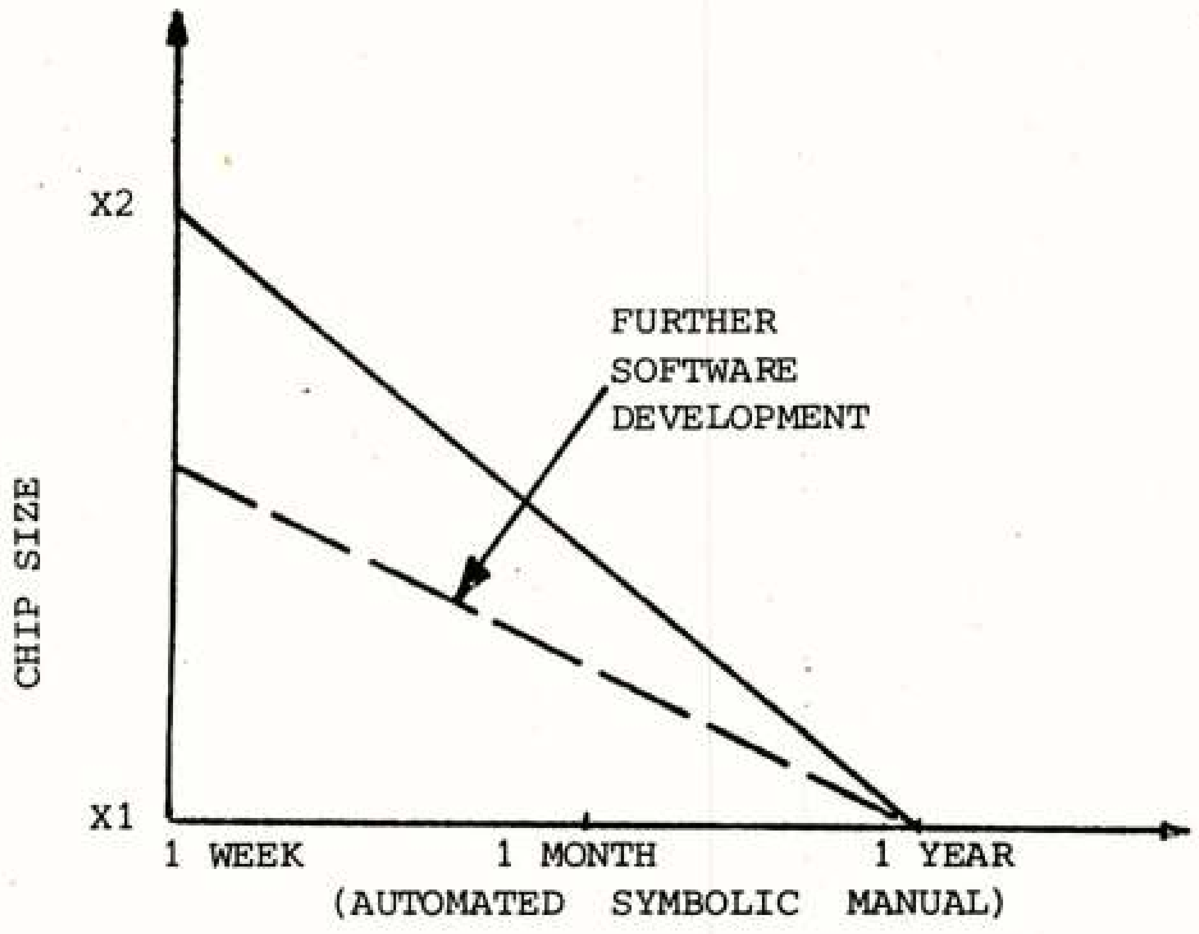


Fig. 6. Chip size vs. layout effort and method.

Invited paper at Esscirc 78
September 1978 in Amsterdam

MICROMACHINED SILICON TRANSDUCERS FOR MEASURING FORCE, PRESSURE, AND MOTION

James B. Angell

Integrated-circuit technology has provided the capability of defining very precise patterns on a silicon surface. When these patterns are used with advanced chemical etching techniques, well defined, very small structures can be formed from a silicon wafer, thereby suggesting a low-cost method of batch fabricating highly uniform, highly repeatable physical shapes. The combination of IC photolithography plus controlled etching of silicon has been labelled "micromachining," because of the inherent precision it provides.

Certain kinds of silicon are highly piezoresistive, in that the resistivity changes very significantly with applied stress. Piezoresistors formed in such silicon enable us to convert mechanically induced stress into an electrical signal. Including piezoresistors into appropriate micromachined silicon shapes thus yields transducers for measuring such physical quantities as acceleration, pressure, and force, as will be described in this paper.

Silicon Micromachining

The heart of silicon micromachining is chemical etching. Two broad categories of silicon etchants are available. Isotropic etchants, such as HF-HNO_3, attack silicon uniformly and tend to etch at the same rate in all directions. Anisotropic etchants, such as potassium hydroxide or hydrazine, etch the (111) planes of single-crystal silicon much more slowly that the other principal crystallographic planes (the difference in etch rate is roughly 100/1). Typical profiles obtained with the two types of etches are shown in Fig. 1.

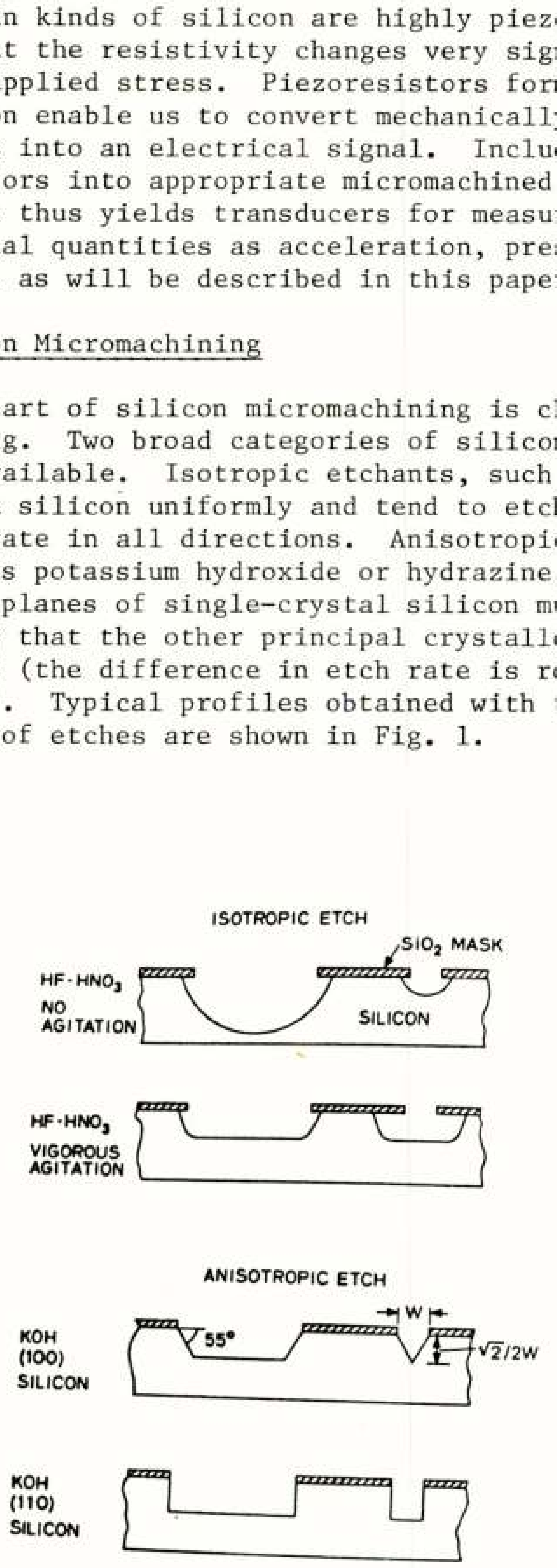


Fig. 1 Etch Profiles in Silicon

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Because the anisotropic etches do not undercut the silicon under the SiO_2 mask to a significant extent, they are usually preferable for precision micromachining, particularly when deep etching is required. Therefore, all the transducers discussed in this paper will be fabricated using anisotropic etches, even though it is not possible to etch accurate circles with them.

The patterns which serve as the etch mask are formed in thermally grown or deposited SiO_2 by standard IC photolithographic steps. The principal precaution which must be observed is to ensure that the SiO_2 is sufficiently thick to endure the etch process, because many etchants, including KOH (which is the most convenient of the anisotropic etchants), slowly etch SiO_2.

A Silicon Accelerometer

The first transducer we will consider is an accelerometer in which the active element is a very thin (15 μm or less) cantilevered beam of silicon[1]. The lower portion of Fig. 2 shows a cross section of the accelerometer. A 200 μm thick silicon mass formed at the free end of the beam serves as the inertial reference. A 200 μm thick silicon supporting rim

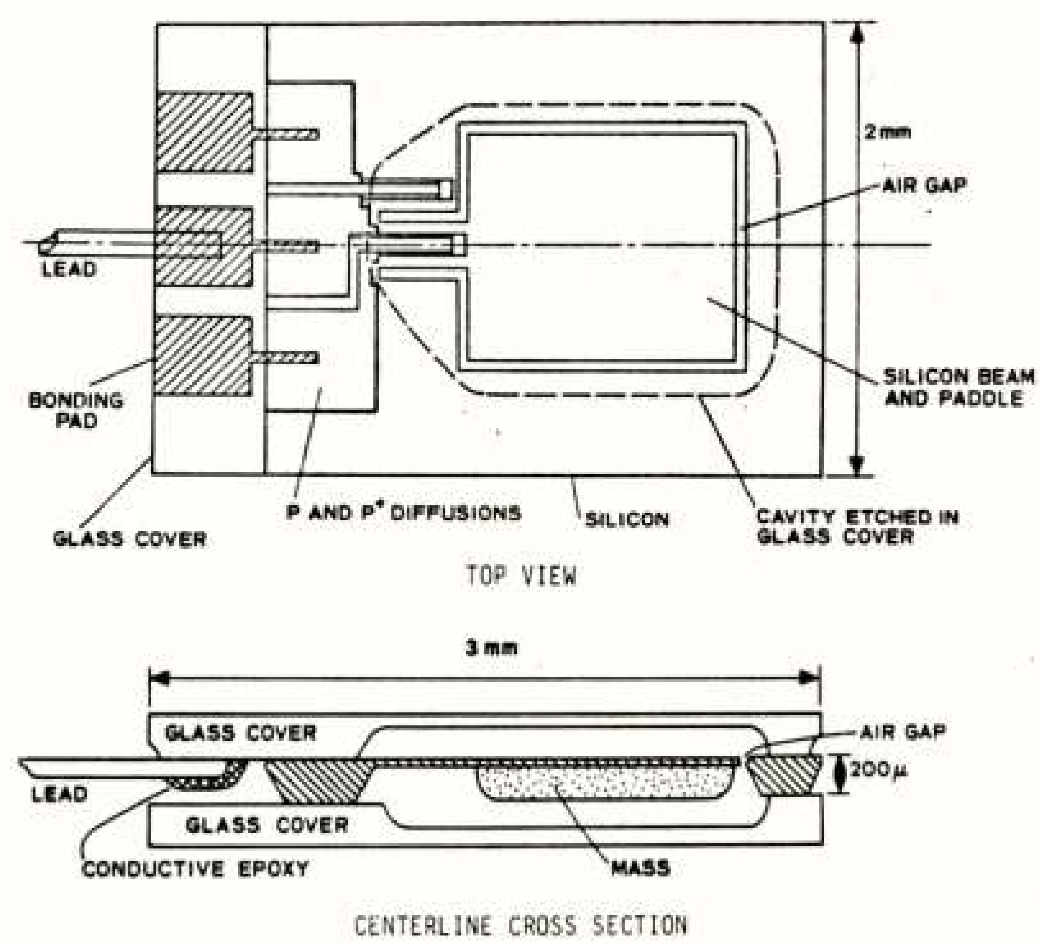


Fig. 2 Top and cross-section views of accelerometer

surrounds the beam and the mass, providing the fixed built-in end condition for the cantilever. Glass covers are bonded to both sides of the supporting rim to provide protection; cavities etched into these covers provide room in which the silicon mass can move. The complete accelerometer package measures 2 x 3 x 0.6 mm, and weighs less than 0.02 gm; this very small mass eliminates measurement artifices which heavier devices might introduce.

This accelerometer is a uniaxial device, measuring acceleration in only one direction, perpendicular to the top surface of the package. The package itself was deliberately designed to give a good reference with respect to the sensitive axis of the accelerometer. With acceleration along this axis,

the mass tends to bend the thin beam, thus causing a stress in the upper surface of the beam which is proportional to acceleration. A lightly doped p-type piezoresistor diffused into the upper surface of the beam changes its resistance in proportion to the stress. A second resistor, located on a nearby unstressed region of thin silicon, provides a temperature dependent reference for externally compensating the temperature dependence of the stress sensitive resistor. The two resistors and the low resistivity p+ diffusion that electrically connects the resistors to the bonding-pad areas are shown in the top view of Fig. 2

The entire fabrication process of both the silicon and the glass covers takes place in wafer form,with 200 accelerometers on a 2-inch wafer. Therefore, the devices should ultimately be inexpensive. The silicon processing steps proceed as follows. First alignment holes are etched through the 200 μm starting n-type silicon wafer from the bottom surface, using a KOH anisotropic etch. Next the p+ and p diffusions are added to the top surface, using conventional photolithography and oxide-masking steps. Then the top surface is covered with a thick layer of SiO_2 and the bottom surface is etched, through an appropriate mask, with KOH to a depth of 170 μm to form the beam, mass, air gap, space for lead attachment and the device separation grooves. A final 15 μm KOH etch from both sides of the wafer completes the formation of the air gap and separation grooves (narrow struts of thick silicon are left in the separation grooves to keep the devices together in wafer form). Fig. 3 shows a view taken with a scanning electron microscope of the bottom of a single chip; the beam, air gap, silicon mass and 55° slopes

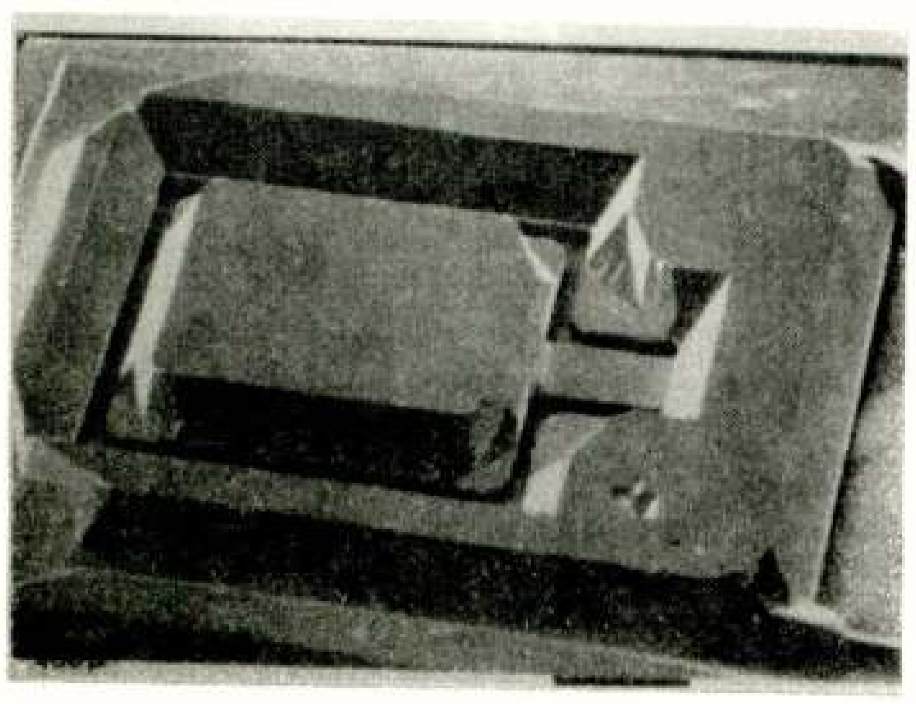


Fig. 3 SEM of the bottom of an accelerometer

of the (111) planes exposed by the anisotropic etch are all clearly evident. The peculiar shape of the outside corners is the result of a different etch rate along the (112) and other higher order crystallographic directions.

The glass caps are made with a Pyrex glass (Corning Glass #7740) with a coefficient of thermal expansion that closely matches that of silicon. The cavities are etched into the glass using a mixture of hydroflouric and nitric acids, with evaporated gold atop evaporated chromium serving as the etch mask. The top glass wafer is next hermetically bonded to the silicon wafer using anodic bonding[2]. In this process, the glass and silicon are brought together, aligned, and heated to 400°C. A 600-volt potential is is applied between the silicon and a metal electrode on the other side of the glass, with the silicon positive. At 400°C, the glass is slightly conductive, due to mobile ions. Therefore, most of the applied voltage appears across a very narrow region at the silicon-glass interface, providing a very high force of attraction and forming an irreversible molecular bond. The bottom glass wafer is then similarly bonded, thus completing the fabrication in wafer form. Finally, the devices are sawn apart with a diamond wheel, and leads are attached to the bonding pads on the top glass cover with a conducting epoxy.

Sensitivities ranging from 2×10^{-4} to 4×10^{-3} $\Delta R/R$ per g have been achieved by varying beam thickness and the size of the mass. A typical device can linearly measure accelerations from 0.01 g to 100 g, and has a resonant frequency of 1000 Hz. Without damping the resonance has a Q of 80 or more; by filling the cavity with isopropyl alcohol (through an etched hole which is later sealed with epoxy) close to critical damping can be achieved.

Silicon Transducer for Measuring Absolute Pressure

Another application of silicon micromachining is a pressure transducer containing a hermetically sealed chamber which provides a stable reference pressure for absolute pressure measurements[3]. This transducer consists of a glass cap which is hermetically sealed, using anodic bonding, to a silicon chip, as shown in Fig. 4. The silicon chip is composed of a

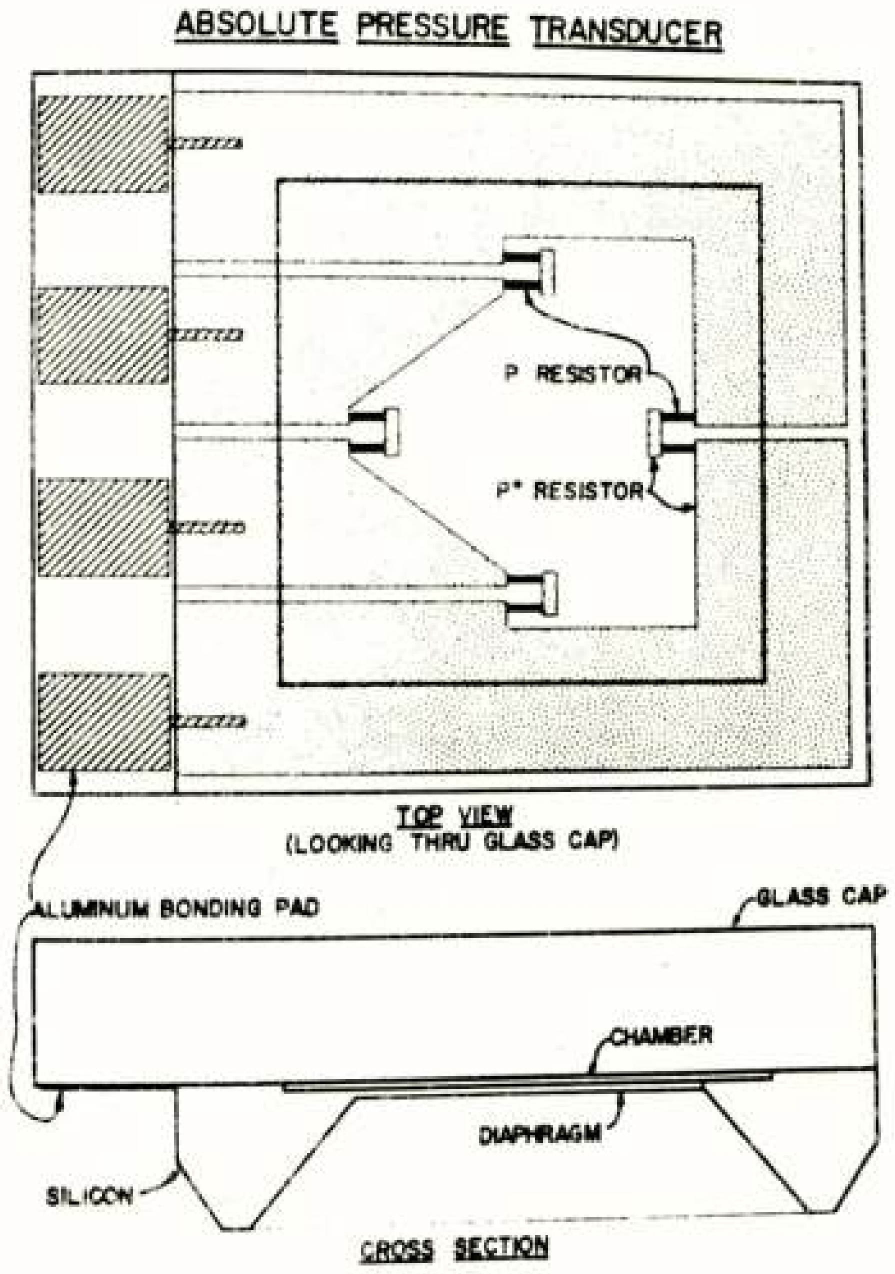


Fig. 4 Absolute pressure transducer

square thin silicon diaphragm (typically 10 μm thick) which is surrounded by a 200 μm thick rim of silicon. The thick rim helps to support and protect the diaphragm. Etched into the top surface of the silicon chip is a well which is 10 μm deep. This well, together with the glass cap, forms the reference pressure chamber.

Four pairs of p-type resistors are diffused into the top surface of the silicon diaphragm at the bottom of the 10 μm well. Each pair of resistors is located at the center of one edge of the diaphragm, at which point the stress caused by a pressure differential applied to the diaphragm is greatest. Two of the resistors are oriented

parallel to the pressure-induced stress, while the other two resistors are perpendicular to the stress. The piezoresistive properties of (110) oriented p-type silicon are such that the resistance change of a resistor oriented perpendicular to the stress is of equal magnitude, but opposite sign, to the change in a parallel resistor. The two resistors of each pair are connected together to form a single resistor by a short section of p+ material. Additional wide p+ regions are used to connect the four resulting resistors together into a Wheatstone bridge, and to connect the Wheatstone bridge to the aluminum bonding pads which are evaporated onto the glass cap

A photograph of an absolute pressure transducer, taken through the glass cap, is shown in Fig. 5. This structure is 1.3 mm long, 1.0 mm wide, and 0.4 mm thick. With a diaphragm 0.5 mm square and

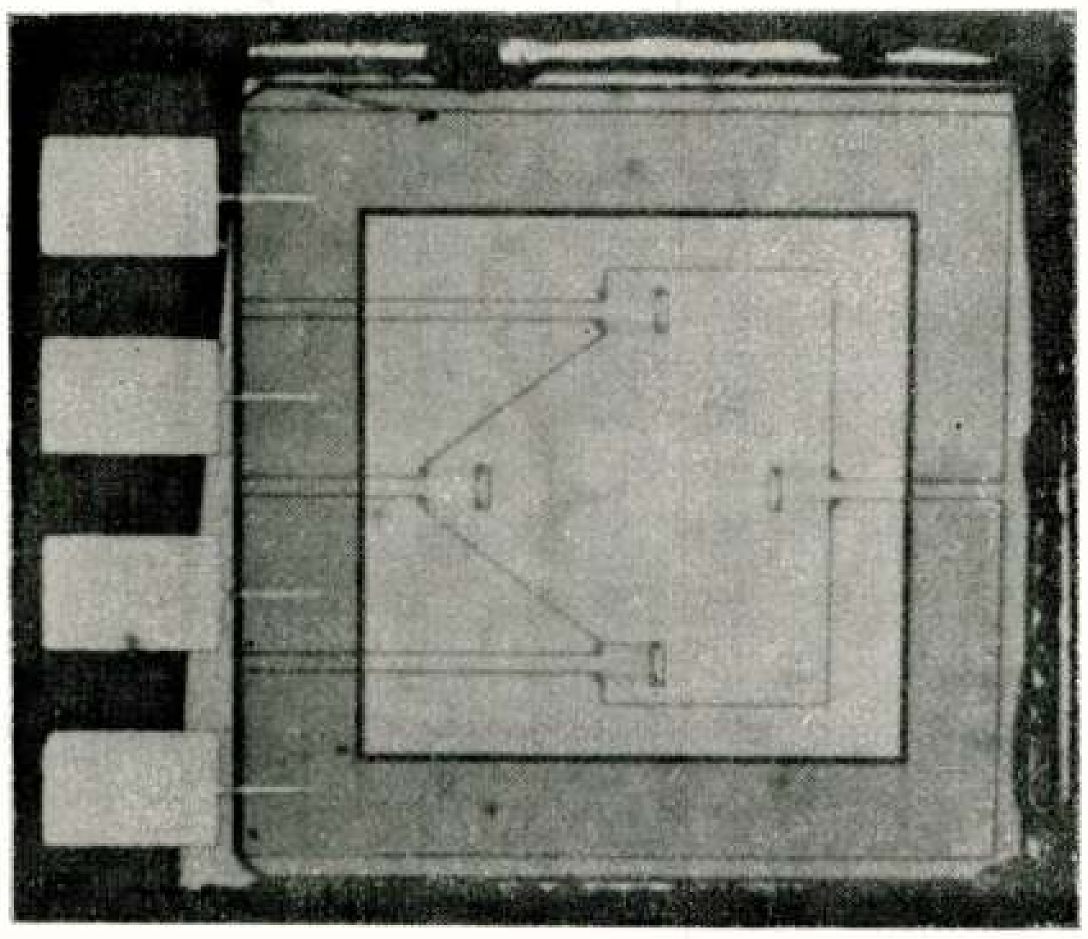


Fig. 5 View through the glass cap of a pressure transducer.

10 μm thick, it has a sensitivity of 30 uV output per volt applied to the bridge per millimeter of mercury pressure difference. No discernible drift in output for a given applied pressure has been observed over a 30-day period.

Temperature changes cause an output voltage change which corresponds to -4 mmHg/°C with a fixed 1-volt supply connected to the Wheatstone bridge. However, if the bridge is driven from a current source, the voltage across the driving point of the bridge varies with temperature, but not with pressure; these variations with temperature can be used to cancel the temperature variations in the bridge output. With this compensation, the output change with temperature is within 0.1 mmHg/°C.

As with the acceleromater, all processing of the absolute pressure transducer up to device separation and lead attachment is in wafer form. Since there are roughly 800 transducers per 2-inch wafer, the pressure transducer is inherently a low-cost structure. While the transducer described here was designed (via size and thickness of the diaphragm) for biomedical applications, it can be optimized as well for other pressure ranges than the 300 mmHg range over which this device is linear.

Force Transducer

A micromachined silicon force transducer, originally developed for in vivo biomedical instrumentation in 1972, is shown in Fig. 6. It is a 1.7 mm long piece of silicon with a stress-sensitive resistor diffused into the middle section. At each end of the resistor are gold bonding pads which make ohmic contacts to the resistor. The silicon ring at each end of the transducer serves as a suture loop for surgical implantation. In the cross section view of Fig. 6 the vertical scale has been expanded 4-to-1 for clarity.

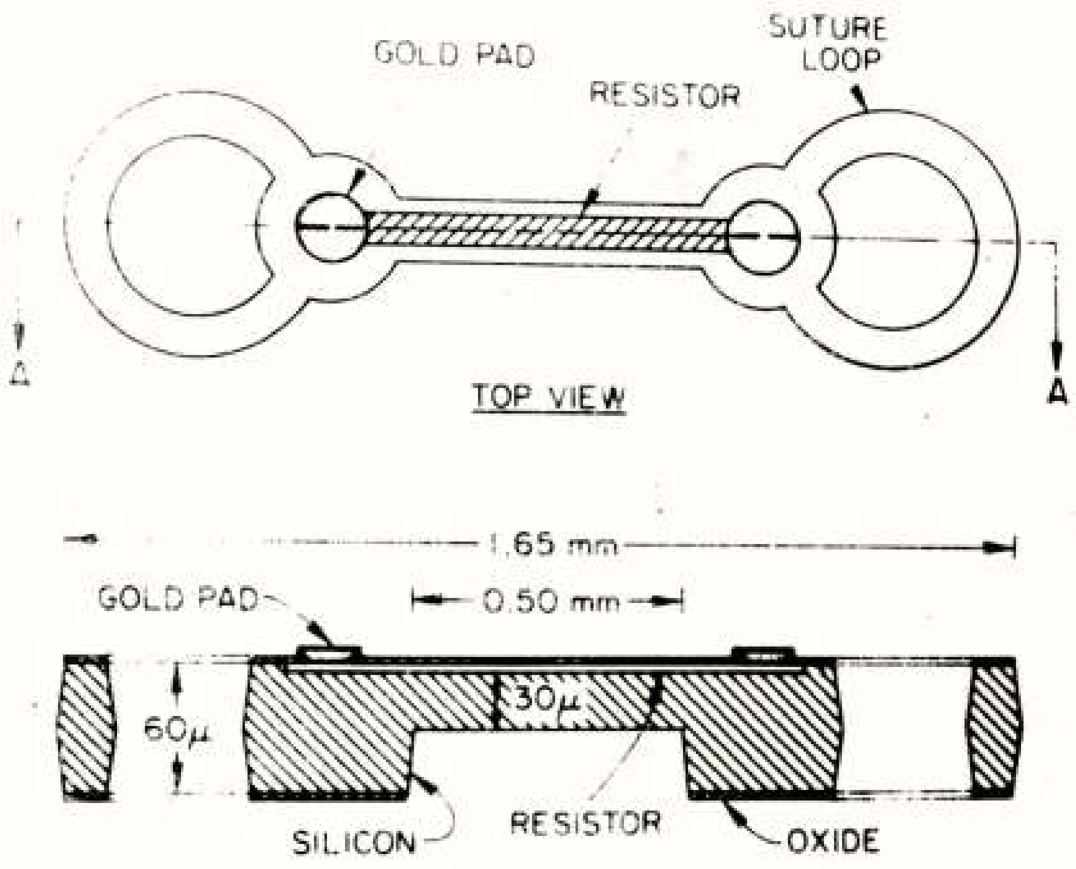


Fig. 6 Force Transducer

The fabrication of these devices begins with a silicon wafer that has been chemically thinned to 60 μm. The processing steps are similar to those described for the accelerometer, and use KOH for the anisotropic etching. The silicon under the piezoresistor is thinned to 30 μm by permitting the KOH to attack only the bottom surface of the silicon, whereas the etchant attacks both top and bottom surfaces to form the suture loops and the perimeter of the device. When the etching of a given device is completed, the device separates from the wafer, falls to the bottom of the etching bath, and is removed. Over 1000 working transducers can normally be obtained from a 2-inch wafer.

These transducers can withstand 90 gm tension or 0.5 gm-cm bending moment before fracturing. At 10% of the breaking stress, the resistor (nominally 1000 ohms) has changed by 3%; up to this point, the resistance change is proportional to stress, with no sign of hysteresis.

Fig. 7 shows a photograph of a completed force transducer; note that the suture loops, which began as circular sectors on the masks, have been distorted by the directional etching characteristics of the anisotropic etchant.

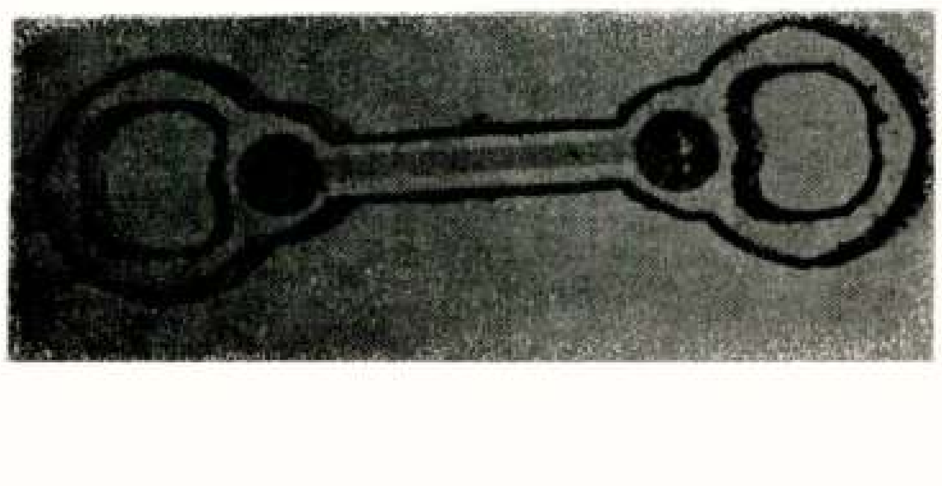


Fig. 7 Microphotograph of a Force Transducer

Lead Attachment and Encapsulation

Attaching electrical leads to transducers has been a major challenge, particularly for biomedical applications, where violent flexing and a highly corrosive environment are present. For accelerometers and force transducers, the leads must also be very flexible; stiff leads would introduce measurement errors. For the force-transducer assemblies, we have achieved greatest reliability using 50 μm platinum-iridium leads attached to the bonding pads with a conductive silver epoxy. In other cases, multistranded copper wire or 25 μm stainless steel wire have served well. The strongest connections, regardless of wire type, have been with conductive epoxy; soldering and thermocompression bonding seem to weaken the adhesion of the bonding pad to the surface supporting it.

Encapsulation with an inert coating is necessary to avoid electrical leakage, corrosive attack of vulnerable areas such as contacts, and possible poisoning of the surroundings (particularly in biomedical applications). For pressure transducers and force transducers the coating must be thin and flexible, so that the calibration of the transducer will not be affected. Typically several layers of different materials are necessary to completely encapsulate a device and achieve protection; however, use of standard insulation materials such as epoxy and silicone rubbers is difficult for these transducers. One promising prospect is a polymer named Parylene, which can be vapor-deposited onto room-temperature surfaces in uniform layers as thin as 0.1 μm[5]. These layers of Parylene are conformal, coating all parts of the transducer and its leads uniformly. 2-μm layers of Parylene do not significantly alter the transduction properties of the devices, and provide short-term moisture protection. However, 15-μm layers are needed to provide a moisture barrier that remains true for 3 months. Thus, work remains in finding a good long-term encapsulation.

The Future

The micromachining technology discussed here is being extended to other devices, and particularly to arrays of sensors so that parameter distributions can be observed. When active circuit elements are included right on the transducer, external leakage currents will become less important and sensor arrays even more convenient. Then, integrated-circuit, micromachined transducers will really have arrived.

References

1) Lynn M. Roylance, "A Miniature IC Accelerometer," 1978 IEEE ISSCC Digest, Feb. 1978, pp220-1.

2) G. Wallis and D.I. Pomerantz, "Field Assisted Glass-Metal Sealing." J. Applied Physics, 40, 3946, 1969.

3) T.A. Nunn "A Silicon Absolute Pressure Transducer for Biomedical Applications," Ph.D. Dissertation, Stanford University, Oct. 1977.

4) T.A. Nunn, J.B. Angell, T.S. Nelsen, "Force Transducer for Oviduct Instrumentation," Proc. Biomed. Eng'g Society, Los Angeles, pp29-30; Jan. 1973.

5) Parylene is a proprietary coating developed by Union Carbide Company

Acknowledgment

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Invited paper at Esscirc 78

September 1978 in Amsterdam

Prof. dr. J. J. Zaalberg van Zelst

Geboren te Amsterdam, 28 september 1911
Overleden te Eindhoven, 27 juli 1978



In de nacht van 26 op 27 juli 1978 is in het Diaconessen ziekenhuis te Eindhoven overleden prof.dr. J.J. Zaalberg van Zelst, gewoon hoogleraar in de elektronica aan de Technische Hogeschool Eindhoven.

Johannes Zaalberg van Zelst werd op 28 september 1911 te Amsterdam geboren. Hij volgde de H.B.S. te Amsterdam en te Hilversum en studeerde natuurkunde aan de Rijks-Universiteit te Utrecht, waar hij in 1935 slaagde voor het doctoraal examen. Nauwelijks een jaar hierna promoveerde hij aan dezelfde universiteit cum laude tot doctor in de wis- en natuurkunde.

Het onderwerp van zijn dissertatie: "Precisie en gevoeligheid van intensiteitsmetingen. Meting van de constante C_1 van Planck" is typerend voor het latere werk van Zaalberg in de fysica en de elektronica. Om met de weliswaar gevoelige maar tegelijk onnauwkeurige elektronische elementen toch aan de extreem hoge nauwkeurigheidseisen te kunnen voldoen die met name bij vele fysische metingen worden verlangd, is voor Zaalberg een voortdurende uitdaging gebleven. Dit heeft niet alleen geresulteerd in een veelheid van ingenieuse schakelingen maar leidde ook tot nog steeds voor de elektronica van groot belang zijnde principes en beschouwingen.

Zo is zijn principe van "Toevoeging van het ontbrekende" in de analoge elektronica zodanig gemeengoed geworden dat vele jongeren in het vakgebied zich nauwelijks meer zullen realiseren dat de meet-elektronica het tientallen jaren zonder deze mogelijkheid heeft moeten stellen. Zijn fundamentele beschouwing over de oscillator als selectieve ruisversterker in plaats van generator van natuurlijke trillingen bracht niet alleen de oplossing voor het probleem van de synchronisatie van elektronische oscillatoren, maar gaf tevens inzicht in het mechanisme van de zuiver fysische oscillatieverschijnselen.

Zijn primaire werk op het Natuurkundig Laboratorium van de N.V. Philips waarbij hij in 1937 in dienst trad en 27 jaar bleef, was er voor alles één van dienstverlening aan met name de fysici en chemici die bij hun onderzoek geconfronteerd werden met de begrenzingen van tot op dat ogenblik bestaande elektronische meetapparatuur. Vrijwel dagelijks werd er een beroep gedaan op zijn uitzonderlijk grote kennis en kunde. In zeer vele gevallen kon hij ter plekke de collega verder helpen, maar uit de veelheid van aangemelde problemen bleven er voldoende over die een beroep deden op zijn als artistiek aan te merken virtuositeit.

Zijn werk vond erkenning ook buiten de kring van het Natuurkundig Laboratorium door zijn benoeming tot bijzonder hoogleraar aan de Rijks Universiteit te Utrecht van wege het Utrechts Universiteitsfonds om onderwijs te geven in de elektronica, welke functie hij van 1958 tot 1968 vervulde. Inmiddels was hij in 1964 benoemd tot gewoon hoogleraar aan de Technische Hogeschool Eindhoven Hij gaf boeiende colleges over elektronische schakelingen vol humorvolle vergelijkingen aan studenten van de afdelingen der Elektrotechniek, Natuurkunde en Werktuigbouwkunde. Met zijn groep - nu vakgroep Elektronische schakelingen - heeft hij het onderwijs in dat vakgebied verzorgd.Talloze studenten hebben stages in zijn

vakgroep uitgevoerd, terwijl bijna 100 studenten daar hun afstudeerwerk hebben verricht. Ook hier wendden vele collega's uit verschillende afdelingen zich tot Zaalberg als zij met moeilijke meetproblemen te kampen hadden. Door de uitwerking en realisering van de ingenieuse oplossingen die hij vaak wist te bedenken op te dragen aan studenten heeft hij op vele jongeren de kennis en vooral ook het enthousiasme voor zijn vak kunnen overbrengen.

Daarnaast moet zeker genoemd worden zijn belangstelling voor het onderwijs in de elektronica in het algemeen. Zo heeft hij ruim 10 jaar zitting gehad in de examencommissies van het NERG en was hij sinds 1950 gecommitteerde namens het NERG bij de hogere-elektronicusexamens van de School voor Elektronica Rens en Rens. Daarmee heeft hij een belangrijke bijdrage tot het elektronica-onderwijs in Nederland geleverd.

Maakte zijn virtuositeit alleen al Zaalberg tot een wel zeer markante persoonlijkheid, het was de dienstbaarheid aan anderen die hem tot een bewonderd en gewaardeerd mens maakte. Hoevelen met moeilijkheden in het werk of anderszins een beroep op hem deden laat zich niet bij benadering schatten, maar in zijn 40 jaren werkzaam leven moeten er vele duizenden zijn geweest. Altijd was Zaalberg bereid zich te verdiepen in de problemen van anderen en te helpen bij het vinden van oplossingen. Dat hij op latere leeftijd steeds meer een vaderfiguur voor zeer vele jongeren werd, was dan ook een vanzelfsprekende ontwikkeling en gaf hem grote bevrediging.

Ondanks het feit dat gedurende een groot deel van de bijna 14 jaar die hij aan de Technische Hogeschool heeft kunnen werken zijn gezondheid werd aangetast door de ziekte die uiteindelijk fataal bleek, wist hij door zijn grote vakkennis gepaard aan een uitzonderlijke eruditie en sociale bewogenheid het respect en de bewondering van zijn collega's, medewerkers en studenten te verkrijgen.

Gezegend met een fenomenaal geheugen en een bijzonder systematische denktrant beschikte Zaalberg niet alleen in zijn primaire werk, maar ook op totaal verschillende terreinen als botanie, kynologie, grafologie, karakterologie over een deskundigheid die slechts aan weinig vakbeoefenaren is gegeven. Deze expertise leidde er weer toe dat ook van buiten zijn directe werkomgeving constant een beroep op hem werd gedaan en ook dat velen hun activiteiten gestimuleerd door Zaalbergs adviezen met meer kans op een gunstig resultaat konden voortzetten.

Met Zaalberg is een nobel mens heengegaan. De droefenis hierover gaat bij hen die hem van nabij hebben meegemaakt gepaard met de dankbaarheid zo'n mens te hebben gekend. Voor zijn vrouw en kinderen moge het een troost zijn te weten dat voor zo velen hun man en vader niet alleen in dankbare herinnering zal blijven, maar ook zijn wijsheid hun handelen zal blijven beïnvloeden.

H.Groendijk
G.Klein

VAN DE REDACTIE

Op verzoek van het internationaal samengestelde "Steering committee" werd door het bestuur van het NERG op 11 november 1976 een commissie ingesteld die de opdracht kreeg in september 1978 een congres Esscirc 78 te organiseren. Dit vierde "European Solid State Circuits Conference" zou worden gehouden in Amsterdam.
Het door het NERG benoemde "Organising committee", waarvan de leden in overleg met het "Steering Committee" werden benoemd, stelde een dagelijks bestuur in, benoemde een "Program Committee" en zocht deelnemers aan een garantiefonds. De namen van de leden van deze committee's en de deelnemers aan het garantiefonds vindt U hieronder.

Het congres zal van 18 tot 21 september 1978 in het Koninklijk Instituut van de Tropen in Amsterdam worden gehouden. Vijf en vijftig sprekers zullen iets over hun laatste werk vertellen. Er zijn reeds 230 aanmeldingen voor deelname binnengekomen. Acht voordrachten worden gehouden op uitnodiging van het "Program Committee". Deze "Invited Papers" zijn in dit nummer afgedrukt; zij zijn overgenomen uit de 205 pagina's tellende "Digest of Technical Papers". De redactie dankt de auteurs en het Program Committee voor de gelegenheid deze te mogen overnemen.

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UIT HET NERG

Personalia

Ter gelegeneid van haar 50 jarig bestaan heeft de CCIR aan een aantal "scientists and engineers" een erediploma gegeven in erkentelijkheid voor exceptionele bijdragen aan de werkzaamheden van deze organisatie. Drie diploma's werden uitgereikt aan nederlanders.

Dr. ir. H.C.A. van Duuren kreeg de onderscheiding voor technische bijdragen en voortdurend leiderschap van studies in radiotelegraphie en radiotelefonie sinds het begin van CCIR en voor zijn voorzitterschap van de studiegroep voor complete systemen van 1948-1970. Dr. ir. H.C.A. van Duuren is lid van onze vereniging sedert 1939.

Prof.dr. F.L. Stumpers ontving het erediploma voor technische bijdragen aan het werk van de CCIR op de gebieden informatietheorie, modulatie en reductie van radiostoringen. Prof.dr.F.L. Stumpers is lid van onze vereniging sedert 1950.

Postuum werd de onderscheiding verleend aan prof.dr. Balth. van der Pol voor: voortdurende technische bijdragen aan het werk van CCIR vanaf de eerste vergadering en eminente verdiensten als eerste directeur van het CCIR van 1949-1957. Prof.dr. Balth van der Pol was een van de oprichters van onze vereniging. Het eerste artikel in dit tijdschrift geschreven, is van zijn hand (1917).

Deze diploma's werden dit voorjaar uitgereikt op de CCIR vergadering in Kyoto.

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